Chapter 20

Assembly and Packaging
Four Important Functions of IC Packaging

1. Protection from the environment and handling damage.
2. Interconnections for signals into and out of the chip.
3. Physical support of the chip.
Traditional Assembly and Packaging

Wafer Test and Sort → Die Separation → Die Attach → Wire Bond → Plastic Package → Final Package and Test
Typical IC Packages

Dual in-line package (DIP)

Single in-line package (SIP)

Thin small outline package (TSOP)

Quad flat pack (QFP)

Plastic leaded chip carrier (PLCC)

Leadless chip carrier (LCC)

Figure 20.2
# Design Constraints for IC Packaging

<table>
<thead>
<tr>
<th>Category</th>
<th>Constraints</th>
</tr>
</thead>
</table>
| **Performance**   | • RC Time delay
                   | • Number of signal I/Os
                   | • Wirebond vs. bump attachment
                   | • Package impedance
                   | • Signal rise time
                   | • Switching transients
                   | • Thermal                                                          |
| **Size/weight/form** | • Chip size
                     | • Package size
                     | • Bond pads size and pitch
                     | • Package leads size and pitch
                     | • Substrate carrier pads size and pitch
                     | • Design of heat sink                                               |
| **Materials**     | • Chip substrate (plastic, ceramic, metal)
                     | • Carrier (organic, ceramic)
                     | • Thermal expansion mismatch
                     | • Lead metallurgy                                                   |
| **Cost**          | • Integration into existing process
                     | • Package materials
                     | • Yield                                                            |
| **Assembly**      | • Method of die attach
                     | • Package attach (through hole, surface mount, bumped)
                     | • Heat sink assembly                                               |
# Levels of IC Packaging

<table>
<thead>
<tr>
<th>First level packaging: IC packaging</th>
<th>Metal leads for mounting onto printed circuit board</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd level packaging: Printed circuit board assembly</td>
<td>Surface-mount chips are soldered on top of tinned pads on the PCB.</td>
</tr>
<tr>
<td>Final product assembly: Final assembly of circuit boards into system</td>
<td>PCB subassembly</td>
</tr>
</tbody>
</table>

- Leads
- Pins
- Edge connector plugs into main system.
- Pins are inserted into holes then soldered on rear of PCB.
Traditional Assembly

- Wafer preparation (backgrind)
- Die separation
- Die attach
- Wire bonding
Schematic of the Backgrind Process

- Downforce
- Rotating and oscillating spindle
- Wafer on rotating chuck
- Table rotates only during indexing of wafers

Figure 20.4
Wafer Saw and Sliced Wafer
Typical Leadframe for Die Attach

Figure 20.6
Epoxy Die Attach

Die

Leadframe

Epoxy

Figure 20.7
Au-Si Eutectic Attach

Figure 20.8
Wires Bonded from Chip Bonding Pads to Leadframe
Wirebonding Chip to Leadframe

Photo 20.1
Thermocompression Bonds

Figure 20.10
Ultrasonic Wirebonding Sequence

(1) Wire

(2) Ultrasonic energy

(3) Tool moves upward. More wire is fed to tool.

(4) Ultrasonic energy

(5) Tool moves upward. Wire breaks at the bond.
Thermosonic Ball Bond

1. Gold wire
2. H2 torch
3. Pressure and ultrasonic energy
4. Tool moves upward and more wire is fed.
5. Pressure and heat form bond.
6. Tool moves upward.

Lead frame

Die

Figure 20.12

Semiconductor Manufacturing Technology
by Michael Quirk and Julian Serda

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Wirebond Pull Test
Traditional Packaging

- Plastic Packaging
- Ceramic Packaging
TO-Style Metal Package
Tie Bar Removal from Leadframe

Figure 20.15
Plastic Dual In-Line Package (DIP) for Pin-In-Hole (PIH)
Single In-Line Package (SIP)
Thin Small Outline Package (TSOP) with Gull wing Surface Mount Leads
Single In-Line Memory Module (SIMM)
Quad Flatpack (QFP) with Gull Wing Surface Mount Leads
Plastic Leaded Chip Carrier (PLCC) with J-Leads for Surface Mount
Leadless Chip Carrier (LCC)
Laminated Refractory Ceramic Process Sequence

Ceramic interconnect layers

4-layer laminate
Ceramic with Pin Grid Array

Courtesy of Advanced Micro Devices
CERDIP Package

- Plane of cross-section
- Indexing notch
- Ceramic lid
- Glass seal
- Metal lead
- Cross-section
- Chip on epoxy and leadframe
- Ceramic base

Figure 20.18
Test Socket for IC Package
Advanced Packaging

- Flip chip
- Ball grid array (BGA)
- Chip on board (COB)
- Tape automated bonding (TAB)
- Multichip modules (MCM)
- Chip scale packaging (CSP)
- Wafer-level packaging
Flip Chip Package

Connecting pin

Substrate

Via

Metal interconnection

Silicon chip

Solder bump on bonding pad

Figure 20.20
C4 Solder Bump on Wafer Bonding Pad

1. Bonding pad
2. 3-layer metal stack: Cu-Sn, Cr+Cu, Cr
3. 2-layer metal deposition: Sn, Pb
4. Solder bumps form during reflow

Reflow Process

Metal Deposition and Etch
Epoxy Underfill for Flip chip

- Solder bump
- Chip
- Epoxy
- Substrate
Flip Chip Area Array Solder Bumps Versus Wirebond
Chip with Ball Grid Array
Ball Grid Array
Chip on Board (COB)
Tape Automated Bonding (TAB)

- Copper leads
- Poyimide tape
Multichip Module (MCM)
Trends for Advanced Packaging

# Diversity of Chip Scale Packages

<table>
<thead>
<tr>
<th>General CSP Approach</th>
<th>CSP Package Name</th>
<th>Company</th>
</tr>
</thead>
<tbody>
<tr>
<td>Custom Leadframe</td>
<td>Area array, bumped CSP</td>
<td>Amkor/Anam</td>
</tr>
<tr>
<td></td>
<td>Small outline no-lead/C-lead (SON/SOC)</td>
<td>Fujitsu</td>
</tr>
<tr>
<td></td>
<td>Bump chip carrier (BCC)</td>
<td>Fujitsu</td>
</tr>
<tr>
<td></td>
<td>Micro-stud-array (MSA)</td>
<td>Hitachi</td>
</tr>
<tr>
<td></td>
<td>Bottom leaded plastic (BLP)</td>
<td>LG Semicon</td>
</tr>
<tr>
<td></td>
<td>Quad flat no-lead (QFN)</td>
<td>Matsushita</td>
</tr>
<tr>
<td></td>
<td>Memory CSP</td>
<td>TI Japan</td>
</tr>
<tr>
<td></td>
<td>Quad outline non-leded</td>
<td>Toshiba</td>
</tr>
<tr>
<td>Interposer (flexible material with interconnects) between die and substrate</td>
<td>Enhanced flex CSP</td>
<td>3M</td>
</tr>
<tr>
<td></td>
<td>FleXBGA</td>
<td>Amkor/Anam</td>
</tr>
<tr>
<td></td>
<td>FBGA</td>
<td>Fujitsu</td>
</tr>
<tr>
<td></td>
<td>Chip-on-flex CSP</td>
<td>GE</td>
</tr>
<tr>
<td></td>
<td>Multi chip scale package (MCSP)</td>
<td>Hightec MC AG</td>
</tr>
<tr>
<td></td>
<td>CSP for memory devices</td>
<td>Hitachi</td>
</tr>
<tr>
<td></td>
<td>IZM flexPAC</td>
<td>Fraunhofer Institute</td>
</tr>
<tr>
<td></td>
<td>Molded Ball Grid Array</td>
<td>Mitsubishi Electric</td>
</tr>
<tr>
<td></td>
<td>Chip-on-flex Chip Size Package</td>
<td>Motorola Singapore</td>
</tr>
<tr>
<td></td>
<td>Fine-pitch BGA (FPBGA)</td>
<td>NEC</td>
</tr>
<tr>
<td></td>
<td>MicroBGA</td>
<td>Tessera</td>
</tr>
<tr>
<td>Rigid Substrate</td>
<td>Chip Array Package (CABGA)</td>
<td>Amkor/Anam</td>
</tr>
<tr>
<td></td>
<td>CSP</td>
<td>Cypress Semiconductor</td>
</tr>
<tr>
<td></td>
<td>Ceramic mini-BGA</td>
<td>IBM</td>
</tr>
<tr>
<td></td>
<td>Molded array process CSP</td>
<td>Motorola</td>
</tr>
<tr>
<td></td>
<td>Plastic chip carrier</td>
<td>National</td>
</tr>
<tr>
<td></td>
<td>CSP</td>
<td>Oki Electric</td>
</tr>
<tr>
<td></td>
<td>Transformed grid array package</td>
<td>Sony</td>
</tr>
<tr>
<td></td>
<td>Ceramic/plastic fine-pitch BGA</td>
<td>Toshiba</td>
</tr>
</tbody>
</table>
Wafer-Level Packaging

Single chip with C4 bumps
C4 Bumped Wafer

Photograph provided courtesy of Advanced Micro Devices
Design Concept for Wafer-Level Packaging

Comparison of Standard Test Flow with Wafer-Level Package Test Flow

Standard Test Flow

- Wafer probe
- Dice wafer
- Package individual ICs
- Socket/burn-in at package level
- Functional test at package level
- Load into tape and reel

WLP Test Flow

- WLP fabrication
- In-situ WLBI
- Wafer-level functional test
- Dicing
- Wafer-level pick at board assembly

Figure 20.31
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package size</td>
<td>The package is equal to the chip size in x and y dimensions. It is the smallest possible IC package and minimizes the package weight.</td>
</tr>
<tr>
<td>Mounted package height</td>
<td>It is extremely thin with a total height &lt; 1.0 mm as measured from the circuit board surface after 2\textsuperscript{nd} level assembly.</td>
</tr>
<tr>
<td>Component reliability</td>
<td>Test results indicate that wafer-level packaging components pass existing reliability tests for passivated components.</td>
</tr>
<tr>
<td>Solder joint reliability</td>
<td>Test results indicated solder joint reliability meets standard thermal cycle (-65 to 125°C) reliability tests.</td>
</tr>
<tr>
<td>Electrical performance</td>
<td>Electrical simulation tests indicates that the die face-down (flip chip) configuration of wafer-level packaging with its short circuit traces results in very good electrical performance for minimizing inductance and parasitic capacitance losses.</td>
</tr>
<tr>
<td>Integration with existing SMT infrastructure</td>
<td>The wafer-level package is compatible with existing surface mount technology and uses standard solder balls and ball pitches.</td>
</tr>
<tr>
<td>Alpha-particle protection</td>
<td>Radioactive elements occurring naturally in packaging materials emit alpha-particles that can cause voltage loss in memory cells. The use of polyimide tape and film adhesive provides alpha-particle protection for memory chips.</td>
</tr>
<tr>
<td>Low system cost</td>
<td>The use of existing materials with wafer integration to reduce handling and a wafer test strategy to minimize duplicate testing provides for a low overall system cost.</td>
</tr>
</tbody>
</table>