Chapter 10

Oxidation
Diffusion Area of Wafer Fabrication

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Oxide Film

• Nature of Oxide Film
• Uses of Oxide Film
  – Device Protection and Isolation
  – Surface Passivation
  – Gate Oxide Dielectric
  – Dopant Barrier
  – Dielectric Between Metal Layers
Atomic Structure of Silicon Dioxide

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### Table 10.1

**Oxide Applications: Native Oxide**

<table>
<thead>
<tr>
<th>Purpose</th>
<th>This oxide is a contaminant and generally undesirable. Sometimes used in memory storage or film passivation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comments</td>
<td>Growth rate at room temperature is 15 Å per hour up to about 40 Å.</td>
</tr>
</tbody>
</table>

- **Silicon dioxide (oxide)**
- **p⁺ Silicon substrate**
Table 10.1
Oxide Applications: Field Oxide

| Purpose: | Serves as an isolation barrier between individual transistors to isolate them from each other. |

**Diagram:**

- Field oxide
- Transistor site
- p⁺ Silicon substrate

**Comments:** Common field oxide thickness range from 2,500 Å to 15,000 Å. Wet oxidation is the preferred method.
### Table 10.1
Oxide Applications: Gate Oxide

<table>
<thead>
<tr>
<th>Purpose:</th>
<th>Serves as a dielectric between the gate and source-drain parts of MOS transistor.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comments:</td>
<td>Growth rate at room temperature is 15 Å per hour up to about 40 Å. Common gate oxide film thickness range from about 30 Å to 500 Å. Dry oxidation is the preferred method.</td>
</tr>
</tbody>
</table>

[Diagram showing a cross-sectional view of a MOS transistor with labeled parts: Gate, Source, Drain, Transistor site, p+ Silicon substrate, and Gate oxide.]
### Table 10.1
Oxide Applications: **Barrier Oxide**

<table>
<thead>
<tr>
<th><strong>Purpose:</strong></th>
<th>Protect active devices and silicon from follow-on processing.</th>
</tr>
</thead>
</table>

**Diagram:**
- **Barrier oxide**
- **Metal**
- **Diffused resistors**
- **p+ Silicon substrate**

**Comments:** Thermally grown to several hundred Angstroms thickness.
### Table 10.1
**Oxide Applications: Dopant Barrier**

<table>
<thead>
<tr>
<th><strong>Purpose:</strong></th>
<th>Masking material when implanting dopant into wafer. Example: Spacer oxide used during the implant of dopant into the source and drain regions.</th>
</tr>
</thead>
</table>

![Diagram of dopant barrier and spacer oxide](image)

**Comments:** Dopants diffuse into unmasked areas of silicon by selective diffusion.
Table 10.1
Oxide Applications: Pad Oxide

<table>
<thead>
<tr>
<th>Purpose</th>
<th>Provides stress reduction for $\text{Si}_3\text{N}_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comments</td>
<td>Thermally grown and very thin.</td>
</tr>
</tbody>
</table>

![Diagram of oxide applications](image-url)
## Table 10.1
### Oxide Applications: Implant Screen Oxide

<table>
<thead>
<tr>
<th>Purpose:</th>
<th>Sometimes referred to as “sacrificial oxide”, screen oxide, is used to reduce implant channeling and damage. Assists creation of shallow junctions.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Comments:</strong></td>
<td>Thermally grown</td>
</tr>
</tbody>
</table>

![Diagram showing ion implantation through screen oxide with high damage to upper Si surface and more channeling compared to low damage with less channeling.](image-url)
### Table 10.1

**Oxide Applications: Insulating Barrier between Metal Layers**

<table>
<thead>
<tr>
<th>Purpose:</th>
<th>Serves as protective layer between metal lines.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Comments:</strong></td>
<td>This oxide is not thermally grown, but is deposited.</td>
</tr>
</tbody>
</table>

![Diagram of oxide application](image)
Thermal Oxidation Growth

• Chemical Reaction for Oxidation
  – Dry oxidation
  – Wet oxidation

• Oxidation Growth Model
  – Oxide silicon interface
    • Use of chlorinated agents in oxidation
  – Rate of oxide growth
  – Factors affecting oxide growth
  – Initial growth phase
  – Selective oxidation
    • LOCOS
    • STI
## Oxide Thickness Ranges for Various Requirements

<table>
<thead>
<tr>
<th>Semiconductor Application</th>
<th>Typical Oxide Thickness, Å</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate oxide (0.18 µm generation)</td>
<td>20 – 60</td>
</tr>
<tr>
<td>Capacitor dielectrics</td>
<td>5 – 100</td>
</tr>
<tr>
<td>Dopant masking oxide</td>
<td>400 – 1,200</td>
</tr>
<tr>
<td></td>
<td>(Varies depending on dopant, implant energy, time &amp; temperature)</td>
</tr>
<tr>
<td>STI Barrier Oxide</td>
<td>150</td>
</tr>
<tr>
<td>LOCOS Pad Oxide</td>
<td>200 – 500</td>
</tr>
<tr>
<td>Field oxide</td>
<td>2,500 – 15,000</td>
</tr>
</tbody>
</table>

*Table 10.2*
Dry Oxidation Time (Minutes)
Wet Oxygen Oxidation

Figure 10.7
Consumption of Silicon during Oxidation

Before oxidation

After oxidation

Figure 10.8
Charge Buildup at Si/SiO2 Interface

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Diffusion of Oxygen Through Oxide Layer

Oxygen supplied to reaction surface

Oxygen-oxide interface

Oxide-silicon interface

$\text{Si}$

$\text{SiO}_2$

$\text{O}, \text{O}_2$

Used with permission from International SEMATECH
Figure 10.12

Linear & Parabolic Stages for Dry Oxidation Growth at 1100ºC

Approximate linear region

Oxidation thickness

Oxidation time (minutes)

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LOCOS Process

1. Nitride deposition

2. Nitride mask & etch

3. Local oxidation of silicon

Cross section of LOCOS field oxide
(Actual growth of oxide is omnidirectional)

4. Nitride strip
Selective Oxidation and Bird’s Beak Effect

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STI Oxide Liner

1. Nitride deposition

2. Trench mask and etch

3. Sidewall oxidation and trench fill

4. Oxide planarization (CMP)

5. Nitride strip

Figure 10.15
Furnace Equipment

- Horizontal Furnace
- Vertical Furnace
- Rapid Thermal Processor (RTP)
## Horizontal and Vertical Furnaces

<table>
<thead>
<tr>
<th>Performance Factor</th>
<th>Performance Objective</th>
<th>Horizontal Furnace</th>
<th>Vertical Furnace</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical wafer loading size</td>
<td>Small, for process flexibility</td>
<td>200 wafers/batch</td>
<td>100 wafers/batch</td>
</tr>
<tr>
<td>Clean room footprint</td>
<td>Small, to use less space</td>
<td>Larger, but has 4 process tubes</td>
<td>Smaller (single process tube)</td>
</tr>
<tr>
<td>Parallel processing</td>
<td>Ideal for process flexibility</td>
<td>Not capable</td>
<td>Capable of loading/unloading wafers during process, which increases throughput</td>
</tr>
<tr>
<td>Gas flow dynamics (GFD)</td>
<td>Optimize for uniformity</td>
<td>Worse due to paddle and boat hardware. Bouyancy and gravity effects cause non-uniform radial gas distribution.</td>
<td>Superior GFD and symmetric/uniform gas distribution</td>
</tr>
<tr>
<td>Boat rotation for improved film uniformity</td>
<td>Ideal condition</td>
<td>Impossible to design</td>
<td>Easy to include</td>
</tr>
<tr>
<td>Temperature gradient across wafer</td>
<td>Ideally small</td>
<td>Large, due to radiant shadow of paddle</td>
<td>Small</td>
</tr>
<tr>
<td>Particle control during loading/unloading</td>
<td>Minimum particles</td>
<td>Relatively poor</td>
<td>Improved particle control from top-down loading scheme</td>
</tr>
<tr>
<td>Quartz change</td>
<td>Easily done in short time</td>
<td>More involved and slow</td>
<td>Easier and quicker, leading to reduced downtime</td>
</tr>
<tr>
<td>Wafer loading technique</td>
<td>Ideally automated</td>
<td>Difficult to automate in a successful fashion</td>
<td>Easily automated with robotics</td>
</tr>
<tr>
<td>Pre-and post-process control of furnace ambient</td>
<td>Control is desirable</td>
<td>Relatively difficult to control</td>
<td>Excellent control, with options of either vacuum or neutral ambient</td>
</tr>
</tbody>
</table>
Horizontal Diffusion Furnace

*Photograph courtesy of International SEMATECH*
Vertical Diffusion Furnace

Photograph courtesy of International SEMATECH

Semiconductor Manufacturing Technology
by Michael Quirk and Julian Serda

Photo 10.2

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Figure 10.16

Block Diagram of Vertical Furnace System
Common Gases used in Furnace Processes

<table>
<thead>
<tr>
<th>Gases</th>
<th>Classifications</th>
<th>Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bulk</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inert gas</td>
<td>Argon (Ar), Nitrogen (N₂)</td>
<td></td>
</tr>
<tr>
<td>Reducing gas</td>
<td>Hydrogen (H₂)</td>
<td></td>
</tr>
<tr>
<td>Oxidizing gas</td>
<td>Oxygen (O₂)</td>
<td></td>
</tr>
<tr>
<td><strong>Specialty</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Silicon-precursor gas</td>
<td>Silane (SiH₄), dichlorosilane (DCS) or (H₂SiCl₂)</td>
<td></td>
</tr>
<tr>
<td>Dopant gas</td>
<td>Arsine (AsH₃), phosphine (PH₃) Diborane (B₂H₆)</td>
<td></td>
</tr>
<tr>
<td>Reactant gas</td>
<td>Ammonia (NH₃), hydrogen chloride (HCl)</td>
<td></td>
</tr>
<tr>
<td>Atmospheric/purge gas</td>
<td>Nitrogen (N₂), helium (He)</td>
<td></td>
</tr>
<tr>
<td>Other specialty gases</td>
<td>Tungsten hexafluoride (WF₆)</td>
<td></td>
</tr>
</tbody>
</table>
Burn Box to Combust Exhaust

Excess combustible gas burns in hot oxygen rich chamber

Combustion chamber (burn box or flow reactor)

Gas from furnace process chamber

Filter

Wet scrubber

Residue

Recirculated water

To facility’s exhaust system

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Thermal Profile of Conventional Versus Fast Ramp Vertical Furnace

The Main Advantages of a Rapid Thermal Processor

- Reduced thermal budget
- Minimized dopant movement in the silicon
- Ease of clustering multiple tools
- Reduced contamination due to cold wall heating
- Cleaner ambient because of the smaller chamber volume
- Shorter time to process a wafer (referred to as cycle time)
# Comparison of Conventional Vertical Furnace and RTP

<table>
<thead>
<tr>
<th>Vertical Furnace</th>
<th>RTP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Batch</td>
<td>Single-wafer</td>
</tr>
<tr>
<td>Hot wall</td>
<td>Cold wall</td>
</tr>
<tr>
<td>Long time to heat and cool batch</td>
<td>Short time to heat and cool wafer</td>
</tr>
<tr>
<td>Small thermal gradient across wafer</td>
<td>Large thermal gradient across wafer</td>
</tr>
<tr>
<td>Long cycle time</td>
<td>Short cycle time</td>
</tr>
<tr>
<td>Ambient temperature measurement</td>
<td>Wafer temperature measurement</td>
</tr>
<tr>
<td>Issues:</td>
<td>Issues:</td>
</tr>
<tr>
<td>Large thermal budget</td>
<td>Temperature uniformity</td>
</tr>
<tr>
<td>Particles</td>
<td>Minimize dopant movement</td>
</tr>
<tr>
<td>Ambient control</td>
<td>Repeatability from wafer to wafer</td>
</tr>
<tr>
<td></td>
<td>Throughput</td>
</tr>
<tr>
<td></td>
<td>Wafer stress due to rapid heating</td>
</tr>
<tr>
<td></td>
<td>Absolute temperature measurement</td>
</tr>
</tbody>
</table>

Table 10.5
Rapid Thermal Processor

Setpoint voltages

Temperature controller

Feedback voltages

Heater head

Wafer

Pyrometer

Axisymmetric lamp array

Reflector plate

Optical fibers

Figure 10.22
RTP Applications

- Anneal of implants to remove defects and activate and diffuse dopants
- Densification of deposited films, such as deposited oxide layers
- Borophosphosilicate glass (BPSG) reflow
- Anneal of barrier layers, such as titanium nitride (TiN)
- Silicide formation, such as titanium silicide (TiSi$_2$)
- Contact alloying
Oxidation Process

• Pre Oxidation Cleaning
  – Oxidation process recipe
• Quality Measurements
• Oxidation Troubleshooting
Critical Issues for Minimizing Contamination

- Maintenance of the furnace and associated equipment (especially quartz components) for cleanliness
- Purity of processing chemicals
- Purity of oxidizing ambient (the source of oxygen in the furnace)
- Wafer cleaning and handling practices
Thermal Oxidation Process Flow Chart

Wet Clean
- Chemicals
- % solution
- Temperature
- Time

Oxidation Furnace
- $O_2$, $H_2$, $N_2$, Cl
- Flow rate
- Exhaust
- Temperature
- Temperature profile
- Time

Inspection
- Film thickness
- Uniformity
- Particles
- Defects

Figure 10.23
# Process Recipe for Dry Oxidation Process

<table>
<thead>
<tr>
<th>Step</th>
<th>Time (min)</th>
<th>Temp (°C)</th>
<th>N₂ Purge Gas (slm)</th>
<th>Process Gas</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>850</td>
<td>8.0</td>
<td>0 0 0</td>
<td>Idle condition</td>
</tr>
<tr>
<td>1</td>
<td>5</td>
<td>850</td>
<td>8.0</td>
<td>0 0 0</td>
<td>Load furnace tube</td>
</tr>
<tr>
<td>2</td>
<td>7.5 Ramp 20°C/min</td>
<td>8.0</td>
<td>0 0 0</td>
<td>Ramp temperature up</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>1000</td>
<td>8.0</td>
<td>0 0 0</td>
<td>Temperature stabilization</td>
</tr>
<tr>
<td>4</td>
<td>30</td>
<td>1000</td>
<td>0</td>
<td>2.5 67 0</td>
<td>Dry oxidation</td>
</tr>
<tr>
<td>5</td>
<td>30</td>
<td>1000</td>
<td>8.0</td>
<td>0 0 0</td>
<td>Anneal</td>
</tr>
<tr>
<td>6</td>
<td>30 Ramp -5°C/min</td>
<td>8.0</td>
<td>0 0 0</td>
<td>Ramp temperature down</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>850</td>
<td>8.0</td>
<td>0 0 0</td>
<td>Unload furnace tube</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>850</td>
<td>8.0</td>
<td>0 0 0</td>
<td>Idle</td>
</tr>
</tbody>
</table>

Note: gas flow units are slm (standard liters per minute) and sccm (standard cubic centimeters per minute)
Wafer Loading Pattern in Vertical Furnace

Calibration parameters:
- Boat size: 160 wafers
- Boat pitch: 0.14 inch
- Wafer size: 8 inches
- Elevator speed: 9.29 cm/min
- Cool down delay: 20 minutes

4 Filler (dummy) wafers
1 Test wafer
75 Production wafers
1 Test wafer
75 Production wafers
1 Test wafer
4 Filler (dummy) wafers

Figure 10.24

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