Analog and Mixed-Signal Design for SOC

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Outline

- Analog and Mixed-Signal Design in the SOC Era
- Current Mirrors and Biasing Circuits
- Single-Stage Amplifiers
- Operational Amplifiers
- Layout of Analog and Mixed-Signal ICs
International Technology Roadmap for Semiconductors (http://public.itrs.net)

Minimum Gate Length for Digital Transistors

Gate Length Projections

Length in nm

2001 2003 2005 2007 2009 2011 2013 2015
ITRS (cont.)

Supply Voltages for Digital and Analog ICs

Supply Voltage Projections

- Analog Supply Range
- Digital Supply Voltage
“The mixed-signal supply voltage continues to lag that of high-performance digital by two or more generations. A combination of multiple gate oxide thickness, multiple thresholds, and DC-DC conversion is needed to support the increased mixed-signal requirements. Solutions in active threshold regulation, substrate biasing, and novel design architecture will be required to extend the trend for lower supply voltages for mixed-signal applications. An alternative to full integration is the SIP that combines circuits made with different technologies and optimized for the desired functions. We expect that full-digital implementations in CMOS will replace most analog functions except for analog-to-digital conversion (ADC).”
Challenges for AMS designers

- Major Issues
  - $g_m$ and $g_o$ are both degrading. $\Rightarrow$ difficult to build high gain amplifiers.
  - Feedback is difficult to use.
  - Signal swing is decreasing with $V_{DD}$. $\Rightarrow$ difficult to get acceptable SNR
  - Many existing architectures will not function
  - Gates are leaking. $\Rightarrow$ Charge redistribution circuits may not work
  - Devices becomes increasingly nonlinear. $\Rightarrow$ Spectral performance of many circuits will degrade.
  - Many existing architectures will not give acceptable performance.
  - Matching is becoming worse. $\Rightarrow$ difficult to obtain acceptable soft yields
  - Performance expectations are increasing.
  - Increased mask and processing costs
  - Increased concerns about AMS test
AMS design in SOC

- Increasing need for data converters
  - Oversampled for low-frequency high resolution
  - Nyquist rate structures for higher speeds
- Feedback will be even more important in high spectral purity applications.
- Design for yield will become essential.
- New circuit architectures that operate at low voltages will become essential.
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MOS Transistors

- **CMOS N-Well Process**

- **Common Used Symbols**
  - NMOS
  - PMOS
MOS Transistors (cont.)

Important Dimensions of a MOS Transistor

- **L**: Channel length
- **W**: Channel width
- **tox**: oxide thickness
- **Capacitance**

\[
C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \text{(oxide capacitance per unit area)}
\]

\[
C_G = C_{ox}WL \quad \text{(gate capacitance)}
\]
MOS Transistors (cont.)

- Drain Current Equation in Saturation Region
  - Including channel-length modulation and body Effects

\[
I_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})
\]

where \( \lambda = \frac{\sqrt{2Kn_{eff}^2}}{\sqrt{qN_{Bt}^2}} \) (L ↑ ⇒ \( \lambda \) ↓)

\[
V_{tn} = V_{tno} + \gamma (\sqrt{V_{SB} + |2\Phi_F|} - |2\Phi_F|)
\]

where \( V_{tno} = V_t \bigg|_{V_{SB}=0} \) and \( \gamma = \frac{\sqrt{2qN_{SCS}^2n_{eff}^2}}{C_{OX}} \) \((V^{1/2})\)

\[
V_{tp} = V_{tpo} - \gamma (\sqrt{V_{BS} + |2\Phi_F|} - |2\Phi_F|)
\]
Small-Signal Model

**Linear Components**

- **Linear Resistor**
  \[ V = RI \]

- **Linear Capacitor**
  \[ Q = CV \]

- **Dependent Circuits**
  \[ I_2 = gV_1 \quad \text{(VCCS)} \]
  \[ V_2 = \alpha V_1 \quad \text{(VCVS)} \]
  \[ I_2 = \beta I_1 \quad \text{(CCCS)} \]
  \[ V_2 = rI_1 \quad \text{(CCVS)} \]

The slope corresponds to resistance, conductance, capacitance, transconductance, etc.
Small-Signal Model (cont.)

Linear Approximation for Nonlinear Components

\[ y(x) = y(x_0) + \frac{dy(x_0)}{dx}(x - x_0) + \frac{d^2 y(x_0)}{dx^2}(x - x_0)^2 + \cdots \]

For small \( \Delta x = x - x_0 \),

\[ \Delta y = y(x) - y(x_0) \approx \frac{dy(x_0)}{dx} \Delta x \]

1. Find the operation point.
2. Determine the slope, which determine the value for the linear component.
3. Remove the DC bias, and replace the device with the linear components.
MOS Small-Signal Model

\[ g_m = \frac{\partial i_D}{\partial v_{GS}} \bigg|_Q = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{tn}) = \sqrt{2\mu_n C_{OX}} \frac{W}{L} I_D = \frac{2I_D}{V_{GS} - V_{tn}} \]

\[ \alpha = r_{ds}^{-1} = g_{ds} = \frac{\partial i_D}{\partial v_{DS}} = \lambda I_D \]

\[ g_{mb} = \frac{\partial i_D}{\partial v_{BS}} \bigg|_Q = \frac{\partial i_D}{\partial v_{tn}} \frac{\partial v_{tn}}{\partial v_{BS}} = \frac{\gamma g_m}{2\sqrt{V_{SB} + 2|\phi_F|}} = \eta g_m \]

\[ V_{in} = V_{mo} + \gamma (\sqrt{V_{SB} + 2\Phi_F} - \sqrt{2\Phi_F}) \]

\[ \frac{\partial V_{in}}{\partial v_{BS}} = -\frac{\gamma}{2} \frac{1}{\sqrt{V_{SB} + 2\Phi_F}} \]
MOS Device Capacitances

- Variation of $C_{GS}$ and $C_{GD}$ versus $V_{GS}$

- Saturation region

$$C_{gs} = \frac{2}{3}C_{ox}WL + C_{ox}L_{ov}W$$
$$C_{gd} = C_{ox}L_{ov}W \text{ (overlap cap.)}$$
$$C_{sb} = (A_s + WL)C_{js} + P_sC_{j-sw}$$
$$C_{db} = A_dC_{jd} + P_dC_{j-sw}$$

$A_s, A_d$ : source and drain areas
$P_s, P_d$ : source and drain perimeters
excluding the side adjacent to the channel
MOS Device Capacitances (cont.)

- **Triode region**

  \[ r_{ds}^{-1} = g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \approx \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{in}) \]

  \[ C_{gs} = \frac{1}{2} C_{OX} W L + C_{OX} L_{OV} W \]

  \[ C_{gd} = \frac{1}{2} C_{OX} W L + C_{OX} L_{OV} W \]

  \[ C_{sb} = (A_s + \frac{1}{2} W L) C_s + P_s C_{j-sw} \]

  \[ C_{db} = (A_d + \frac{1}{2} W L) C_{jd} + P_d C_{j-sw} \]

- **Cut-off region**

  \[ C_{gs} = C_{OX} L_{OV} W \]

  \[ C_{gd} = C_{OX} L_{OV} W \]

  \[ C_{sb} = A_s C_s + P_s C_{j-sw} \]

  \[ C_{db} = A_d C_{jd} + P_d C_{j-sw} \]

  \[ C_{gb} = \frac{W L C_{OX} C_{depl}}{W L C_{OX} + C_{depl}} \]
Basic Current Mirrors

- **MOSFETs as Current Source**
  - Biasing in **saturation** with a fixed gate voltage

  \[ V_b = \frac{R_2}{R_1 + R_2} V_{DD} \]

  \[ I_{out} = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_b - V_{tn})^2 (1 + \lambda V_{eff}) \]

- Using resistive divider to provide the gate voltage

  Sensitivity to supply, process and temperature
Basic Current Mirrors (cont.)

Current Copiers

- Diode-Connected device providing inverse function
  
  Assume $\lambda=0$.  

\[ I_D = f(V_{GS}) \]
\[ V_{GS} = f^{-1}(I_{REF}) \]

\[ I_{REF} = \frac{1}{2} \mu_n C_{OX} \left( \frac{W}{L} \right)_1 (V_{GS} - V_{in})^2 \]
\[ I_{out} = \frac{1}{2} \mu_n C_{OX} \left( \frac{W}{L} \right)_2 (V_{GS} - V_{in})^2 \]
\[ I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \]
Errors in Current Mirrors

Simple Current Mirror

M2 in saturation region:
\[ V_{out} \geq V_{GS} - V_{in} = V_{eff} \]
\[ I_{out} = \frac{(W / L)_2}{(W / L)_1} \frac{1 + \lambda V_{eff}^2}{1 + \lambda V_{eff}^1} \times I_{in} \]

Output resistance

\[ R_{out} = r_{ds2} \]
Cascode Current Mirror

- Suppressing Channel-Length Modulation Effect
  ⇒ cascode structure

- Output Resistance

\[ R_{out} \approx (g_{m3}r_{ds3})r_{ds2} \]
Cascode Current Mirror (cont.)

- Head-room consumed by a cascode mirror

\[ V_N = V_{GS0} + V_{GS1} = \sqrt{\frac{2I_{REF}}{\mu C_{OX}(W/L)_0}} + V_{tn0} + \sqrt{\frac{2I_{REF}}{\mu C_{OX}(W/L)_0}} + V_{tn1} \]

\[ V_{out} \geq V_N - V_{tn3} = V_{eff0} + V_{eff1} + V_{tn1} \]
Cascode Current Mirror (cont.)

- Minimum headroom voltage

\[ V_b = 2V_{GS} - V_{in} \]

\[ V_b = 2V_{GS} \]
Low-Voltage Cascode Current Mirror

- Modified of Cascode CM for Low-Voltage (Wide-Swing) Operation

M2 in saturation:
\[ V_X = V_{GS1} \geq V_b - V_{m2} \Rightarrow V_b \leq V_{GS1} + V_{m2} \]

M1 in saturation:
\[ V_A = V_b - V_{GS2} \geq V_{GS1} - V_{m1} \Rightarrow V_b \geq V_{GS1} + V_{GS2} - V_{m1} \]
\[ \Rightarrow V_{GS1} + V_{GS2} - V_{m1} \leq V_b \leq V_{GS1} + V_{m2} \]
\[ \Rightarrow V_{GS1} + V_{GS2} - V_{m1} \leq V_{GS1} + V_{m2} \]
\[ \Rightarrow V_{GS2} - V_{m1} \leq V_{m2} \]

\[
V_b = (V_{GS1} - V_{m1}) + V_{GS2} \\
\Rightarrow V_{out} \geq V_b - V_{m2} = V_{eff1} + V_{eff2}
\]
Biased by a diode-connected transistor

\[
\begin{align*}
\frac{W}{L}_1 &= \frac{W}{L}_3 = \frac{W}{L} \\
\frac{W}{L}_2 &= \frac{W}{L}_4 = \frac{1}{n^2} \frac{W}{L} \\
\frac{W}{L}_5 &= \frac{1}{(n+1)^2} \frac{W}{L}
\end{align*}
\]

Let \( I_1 = I_{REF} \).

Then, \( V_{\text{eff}} = V_{\text{eff}1} = V_{\text{eff}3} = \sqrt{\frac{2I_{\text{REF}}}{\mu_n C_{OX} \frac{W}{L}}} \)

Inaccuracy due to

- Body effect
- Some margin is necessary to ensure saturation.

\( \Rightarrow \) Reduce the aspect ratio for M5.

and \( V_b = (n+1)V_{\text{eff}} + V_{m5} = V_{\text{eff}1} + V_{\text{eff}2} + V_{m5} \)
Low-Voltage Cascode Current Mirror (cont.)

- Design for short-Channel Devices

![Diagram of a cascode current mirror with labeled components and a graph showing the relationship between input and output voltage.]
Regulated Drain Current Mirror

Added amplifier to increase output resistance.

Beta-multiplier from Fig. 20.22 (Table 9.2)

NMOS are 50/2.
PMOS are 100/2.
Supply-Independent Bias

Supply-Dependent Biasing

- Resistive Bias

\[ \Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \left( \frac{W}{L} \right)_2 \]

⇒ sensitive to \(V_{DD}\)

Example
Supply-Independent Biasing (cont.)

- Using MOSFET only

\[ V_{DD} = \frac{2I_{REF}}{\mu C_{OX}\left(W/L\right)_{n}} + V_{tn} + \frac{2I_{REF}}{\mu C_{OX}\left(W/L\right)_{p}} - V_{tp} \]
Supply-Independent Biasing (cont.)

Supply-Independent Biasing

Example for Long-channel devices

\[
V_{DD} \quad M_1, 10/2 \quad M_2, 40/2 \quad M_3, 30/2 \quad M_4, 30/2
\]

Start-up circuit (important)

\[
I_{out} = \frac{2}{\mu_n C_{OX} (W/L)_N} \cdot \frac{1}{R_B} \left(1 - \frac{1}{\sqrt{K}}\right)^2
\]

Neglect the body effect.

\[
\sqrt{\frac{2I_{out}}{\mu_n C_{OX} (W/L)_N}} + V_{tn1} = \sqrt{\frac{2I_{out}}{\mu_n C_{OX} K(W/L)_N}} + V_{tn2} + I_{out} R_B
\]
Supply-Independent Biasing (cont.)

- Short-Channel Device

![Diagram of short-channel device with labels and symbols.]

See Table 9.2.
Supply-Independent Biasing (cont.)

- Using feedback to increase the output resistance of MOSFET

Modelled in SPICE using a voltage-controlled voltage source.

\[ V_{bias} = 10 \cdot (V_{reg} - V_{biasn}) \]
Supply-Independent Biasing (cont.)

- Improved circuit

(a) MCP and MCN not present
(b) MCP and MCN present

What happens when VDD is pulsed from 0 to 1 at 50 ns.
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Common-Source Amplifier

\[ A_{v0} = -g_{m1} R_{out} \]

\[ \omega_{-3dB} \approx \frac{1}{R_{in}[C_{gs1} + C_{gd1}(1 + g_{m1} R_{out})] + R_{out}(C_{gd1} + C_2)} \]

\[ \omega_p^2 \approx \frac{g_{m1} C_{gd1}}{C_{gd1} C_{gs1} + C_{gs1} C_2 + C_{gd2} C_2} \]

\[ D(s) = (1 + \frac{s}{\omega_p}) (1 + \frac{s}{\omega_p^2}) \approx 1 + \frac{s}{\omega_p} + \frac{s}{\omega_p^2} \]

\[ R_{out} = r_{ds1} // r_{ds2} \]

\[ C_2 = C_L + C_{dh1} + C_{db2} \]

\[ V_{out} = \frac{-g_{m1} R_{out} (1 - s C_{gd1} / g_{m1})}{V_{in} (1 + sa + s^2 b)} \]

where

\[ a = R_{in}[C_{gs1} + C_{gd1}(1 + g_{m1} R_{out})] + R_{out}(C_{gd1} + C_2) \]

\[ b = R_{in} R_{out}(C_{gd1} C_{gs1} + C_{gs1} C_2 + C_{gd2} C_2) \]
**Common-Source Amplifier (cont.)**

- **Miller’s Theorem**

  ![Miller’s Theorem Diagram]

  \[ I_1 = (V_1 - V_2)Y = V_1(1 - K)Y = V_1Y \]

  \[ I_2 = (V_2 - V_1)Y = V_2(1 - \frac{1}{K})Y = V_2Y \]

  \[ Y_1 = (1 - K)Y \]

  \[ Y_2 = (1 - \frac{1}{K})Y \]

- **Miller Capacitance**

  \[ K = A_{v0} = -g_m R_{out} \]

  \[ C_M = C_{left} = (1 - K)C_{gd1} = (1 + g_m R_{out}) C_{gd1} \]

  \[ \approx g_m R_{out} C_{gd1} \quad \text{(Miller Capacitor)} \]

  \[ C_{right} = (1 - \frac{1}{K})C_{gd1} \approx C_{gd1} \quad \text{(usually neglected)} \]

- **-3dB Frequency**

  - **open-circuit time constant method**

  \[ \omega_{3dB} \approx \frac{1}{\sum_i R_i C_i} \approx \frac{1}{R_{in}[C_{gs1} + C_M] + R_{out}(C_{right} + C_2)} \]
Source Follower

- No voltage gain
- Low output resistance
- Not suffering from Miller effect ⇒ better frequency response
- Exhibiting large amounts of overshoot and ringing under certain conditions

\[ R_2 = r_{ds1} \parallel r_{ds2} \parallel \left( \frac{1}{g_{s1}} \right) \]
\[ C_2 = C_L + C_{sb1} + C_{db2} \]
\[ R_{out} = R_2 \parallel \left( \frac{1}{g_{m1}} \right) = \left( g_{m1} + g_{s1} + g_{ds1} + g_{ds2} \right)^{-1} \approx 1/g_{m1} \]
\[ A_{v0} = g_{m1} R_{out} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} < 1 \]
**Common-Gate Amplifier**

- The gain is slightly less than that of the common-source amplifier.
- Since the gate of the transistor is ac ground, it does not suffer from Miller effect.
  
  ⇒ Frequency response is superior to that of CS amplifier.
Cascode Amplifier

Folded-Cascode Amplifier
⇒ improving input range

For $R_{in} \ll R_{out}$, the -3dB frequency is usually dominant by the output pole due to its large output resistance.

$$\omega_{-3dB} \approx \frac{1}{R_{out}C_L}$$
Differential Amplifier

Differential Pair

\[ i_{D1} \quad i_{D2} \]

\[ v_{ii} \rightarrow \text{M1} \rightarrow \text{M2} \rightarrow 2.5V \]

\[ i_B \]

\[ v_{ii} \uparrow \text{then} \quad i_{D2} \downarrow \]

\[ v_{ih} \uparrow \text{then} \quad i_{D1} \uparrow \]
Differential Amplifier (cont.)

Current Mirror Load -- Large-Signal Analysis

\[ V_{out} = f(V_{in1} - V_{in2}) \]

\[
\begin{align*}
V_{out} &= I_S (V_{in1} - V_{in2}) \\
&= \frac{I_S}{2} (V_{in1} - V_{in2}) + \frac{I_S}{2} (V_{in1} - V_{in2}) \\
&= \left( \frac{I_S}{2} + \frac{I_S}{2} \right) (V_{in1} - V_{in2}) \\
&= I_S (V_{in1} - V_{in2})
\end{align*}
\]

\[
\begin{align*}
V_{out} &= I_S (V_{in1} - V_{in2}) \\
&= \frac{I_S}{2} (V_{in1} - V_{in2}) - \frac{I_S}{2} (V_{in1} - V_{in2}) \\
&= \left( \frac{I_S}{2} - \frac{I_S}{2} \right) (V_{in1} - V_{in2}) \\
&= 0
\end{align*}
\]

M₁, M₃, M₄: off
M₂, M₅: deep triode

\[ V_{out} = 0 \]
Differential Amplifier (cont.)

- I/O Characteristic

- $V_{out}$ vs. $V_{DD}$

For symmetric circuit, $V_{out} = V_F$
Differential Amplifier (cont.)

- Small-Signal Analysis
  - Asymmetric Swings due to the Load

- Calculation of Gm

\[
G_m = \frac{i_{out}}{v_{in}} = -g_{m1}
\]

\[
i_{out} = -g_{m1} \frac{v_{in}}{2} - g_{m2} \frac{v_{in}}{2} = -g_{m1}v_{in}
\]
Differential Amplifier (cont.)

- **Calculation of $R_{out}$**

\[
I_X = 2 \left( \frac{V_X}{2r_{o1,2}} + \frac{1}{g_{m3}} \right) \approx \frac{V_X}{r_{o4} + r_{o1,2}} + \frac{V_X}{r_{o4}}
\]

\[R_{out} \approx r_{o2} // r_{o4}\]

- **Overall Gain**

\[g_{m1} = \sqrt{\frac{\mu_n C_{OX}}{L}} \frac{W}{I_{bias}}\]

\[r_{ds2} = \frac{2}{\lambda M_2 I_{bias}}\]

\[r_{ds4} = \frac{2}{\lambda M_4 I_{bias}}\]

\[R_{out} = r_{ds2} // r_{ds4}\]

\[C_2 = C_L + C_{db2} + C_{db4}\]

\[A_{v0} \approx g_{m1} R_{out}\]

\[\omega_{3dB} \approx \frac{1}{R_{out} C_2}\]
Differential Amplifier (cont.)

- Single-Ended vs Differential Amplifier

For given device dimension, this circuit requires half of the bias current to achieve the same gain as a differential pair. However, advantages of differential operation often outweigh the power penalty.

\[ A_v = -g_{m1} \left( \frac{r_{o1}}{r_{o2}} \right) \]
Differential Amplifier (cont.)

Power-Supply Rejection Ratio (PSRR)

\[ A_{dd} = 1 \Rightarrow \text{PSRR}_+ = \frac{A_d}{A_{dd}} = A_v \]

\[ A_{ss} = \frac{v_o}{v_{ss}} = 0 \]

\[ \text{PSRR}_- = \left| \frac{A_d}{A_{ss}} \right| \rightarrow \infty \Rightarrow \text{mainly due to mismatches} \]
Systematic Design Approach

Parameter Domains for Characterizing Amplifier Performance

- Degrees of Freedom: 2
  - Small-signal parameter domain \( \{g_m, r_o\} \)
    \[
    A_v = -g_m r_o \quad GB = \frac{g_m}{C_L}
    \]
  - Natural design parameter domain \( \{W/L, I_D\} \)
    \[
    A_v = -\left[ \frac{\sqrt{2\mu_n C_{OX}}}{\lambda} \right] \frac{\sqrt{W/L}}{\sqrt{I_D}} \quad GB = \left[ \frac{\sqrt{2\mu_n C_{OX}}}{\lambda} \right] \sqrt{W/L} \sqrt{I_D}
    \]
  - Alternate parameter domain \( \{P, V_{EB}\} \)
    \[
    A_v = -\left[ \frac{2}{\lambda} \right] \frac{1}{V_{EB}} \quad GB = \left[ \frac{2}{V_{DD}C_L} \right] \frac{P}{V_{EB}}
    \]
**Systematic Design Approach (cont.)**

### Design Equations

- **Excess bias:**
  
  \[ V_{EB} = V_{GS} - V_m \text{ or } V_{SGp} + V_p \]

- Let \( I_{DS} = \alpha I_B \)  \( \Rightarrow P = V_{DD} (1 + \alpha) I_B \)  \( \Rightarrow I_{D1,2} = \frac{I_{DS}}{2} = \frac{\alpha P}{2V_{DD} (1 + \alpha)} \)

- **Output resistance:**
  
  \[ R_{out} = \frac{r_{ds1}}{2//r_{ds4}} = \frac{1}{(\lambda_n + \lambda_p)I_{D1}} = \frac{2V_{DD} (1 + \alpha)}{\alpha P(\lambda_n + \lambda_p)} \]

- **Gain:**
  
  \[ A_v = g_m R_{out} = \frac{\mu C_S (\frac{W}{L}) V_{EB1}}{(\lambda_n + \lambda_p)(\frac{1}{2} \mu C_S (\frac{W}{L}) V_{EB1}^2)} = \frac{2}{(\lambda_n + \lambda_p)V_{EB1}} \]

- **Phase margin:**
  
  \[ PM \approx 180 - \tan^{-1} \left( \frac{\omega_i}{\omega_p1} \right) \]

\[ SR = I_{DS} \frac{C_L}{V_{EB1} GB} \]

\[ V_{out(max)} = V_{DD} - V_{EB1} - V_{EB1} \]

\[ V_{out(min)} = V_{EB3} \]
Systematic Design Approach (cont.)

- **Input Common-Mode Range (CMR)**

  - **CMR+**
    
    For M5 in the saturation region,
    \[
    V_{SD5_{\text{(min)}}} = V_{EB5}
    \]
    \[
    V_{CM+} = V_{DD} - V_{EB5} - V_{SG1} = V_{DD} - V_{EB5} - V_{EB1} - V_{tp1}
    \]

  - **CMR-**
    
    For M1 in the saturation region,
    \[
    V_{SD1} \geq V_{SG1} + V_{tp1} \quad \Rightarrow \quad V_{G1} \geq V_{D1} + V_{tp1} = V_{GS3}
    \]
    \[
    V_{CM-} = V_{GS3} + V_{tp1} = V_{EB3} + V_{m3} + V_{tp1}
    \]
## Spread Sheet Method

<table>
<thead>
<tr>
<th>L=1μm, W=10μm, VDS=0.825V and ID=100μA</th>
</tr>
</thead>
</table>

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<th>VEB1</th>
<th>VEB3</th>
<th>VBE5</th>
<th>$A_v$</th>
<th>$A_v$ (dB)</th>
<th>GB (Hz)</th>
<th>$R_{out}$</th>
<th>$f_{p1}$ (Hz)</th>
<th>PM</th>
<th>SR (V/us)</th>
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<td>1.23E-04</td>
<td>0.57</td>
<td>0.105</td>
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<th>$V_{icm}(\text{max})$</th>
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<th>$I_{B}$</th>
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Outline

- Analog and Mixed-Signal Design in the SOC Era
- Current Mirrors and Biasing Circuits
- Single-Stage Amplifiers
- Operational Amplifiers
- Layout of Analog and Mixed-Signal ICs
Ideal Opamps and Applications

**Ideal Opamp**

\[ V_{OUT} = A(V_{IN}^+ - V_{IN}^-) \]

- \( R_{id} \to \infty \)
- \( R_o \to 0 \)
- \( A \to \infty \)
- \( BW \to \infty \)

**Open Loop**

slope = A
Ideal Opamps and Applications (cont.)

- Close Loop with Negative Feedback

\[ V_{IN}^+ - V_{IN}^- = \frac{V_{OUT}}{A} \]

For \( A \to \infty \) and negative feedback, \( V_{IN}^+ - V_{IN}^- = 0 \).

- Inverting amplifier

\[ V_{IN} = -\frac{V_{OUT}}{R_1} \]

\[ \Rightarrow \frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1} \]

- Finite open-loop gain

\[ V_{IN} + \frac{V_{OUT}}{A} = \frac{V_{OUT}}{R_1} - \frac{V_{OUT}}{R_2} \]

\[ \Rightarrow \frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1} \times \frac{1}{1 + (1 + \frac{R_2}{R_1}) / A} \]
Ideal Opamps and Applications (cont.)

- **Non-inverting amplifier**
  
  ![Non-inverting amplifier diagram]

  \[
  \frac{-V_{IN}}{R_1} = \frac{V_{IN} - V_{OUT}}{R_2} \\
  \Rightarrow V_{OUT} = \frac{1}{V_{IN}} + \frac{R_2}{R_1}
  \]

- **Difference amplifier**

  ![Difference amplifier diagram]

  For \( R_1 = R_3 \) and \( R_2 = R_4 \),

  \[
  V_{OUT} = \frac{R_2}{R_1} (V_2 - V_1)
  \]
Stability

General Considerations

- Basic negative-feedback system

\[ Y(s) = \frac{H(s)}{1 + \beta H(s)} \]

Loop gain: \( L(s) = \beta H(s) \)
Assume \( \beta \) is frequency in dependent and \( \beta \leq 1 \).

Example

\[ \beta = \frac{R_1}{R_1 + R_2} \quad \Rightarrow \quad \frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} = \frac{1/\beta}{1 + 1/(A\beta)} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + (1 + \frac{R_2}{R_1})/A} \]

If \( A\beta >> 1 \),
\[ \frac{V_{OUT}}{V_{IN}} \approx \frac{1}{\beta} = 1 + \frac{R_2}{R_1}. \]
Stability (cont.)

论证 Barkhausen’s Criteria for oscillation

\[ |L(j\omega_0)| = 1 \]
\[ \angle L(j\omega_0) = -180^\circ \Rightarrow \text{The system oscillates at } \omega_0. \]

Example

\[
L(s) = -(1 + \frac{R_2}{R_1}) \frac{Z_p}{Z_p + Z_s} = -\frac{1 + R_2 / R_1}{3 + sCR + 1/(sCR)}
\]

\[
L(j\omega) = -\frac{1 + R_2 / R_1}{3 + j[\omega CR - 1/(\omega CR)]}
\]

\[ \angle L(j\omega_0) = 180^\circ \Rightarrow \omega_0 CR - 1/(\omega_0 CR) = 0 \]

\[ \Rightarrow \omega_0 = \frac{1}{RC} \]

\[ |L(j\omega_0)| = 1 \Rightarrow R_2 / R_1 = 2 + \delta \]
Stability (cont.)

- Bode plot of loop gain for unstable and stable system

System is unstable, if
\[ |L(j \omega_{-180})| > 1 \] excess gain
\[ \angle L(j \omega_{0dB}) < -180^\circ \] excess phase

System is stable, if
\[ |L(j \omega_{-180})| < 1 \]
\[ \angle L(j \omega_{0dB}) > -180^\circ \]

\( \omega_{0dB} \): gain crossover point (GX)
\( \omega_{-180} \): phase crossover point (PX)
Stability (cont.)

- **Time-domain responses versus the pole locations**

\[ p = \sigma_p + j\omega_p \Rightarrow \exp(\sigma_p + j\omega_p)t \]

**RHP poles**
Unstable with growing amplitudes

**Imaginary poles**
Unstable with constant-amplitude oscillation

**LHP poles**
\( \Rightarrow \) stable
Stability (cont.)

- **One-pole system**

\[ H(s) = \frac{A_0}{1 + s / \omega_0} \]

\[ \frac{Y}{X}(s) = \frac{A_0}{1 + A_0 \beta} \frac{1}{1 + s / [(1 + A_0 \beta) \omega_0]} \]

\[ p = -(1 + A_0 \beta) \omega_0 \]

\[ \Rightarrow \text{unconditional stable} \]
Stability (cont.)

Multipole Systems

Two-pole system

\[
H(s) = \frac{A_0}{(1 + s / \omega_{p1})(1 + s / \omega_{p2})}
\]

\[
\frac{Y}{X}(s) = \frac{A_0}{(1 + s / \omega_{p1})(1 + s / \omega_{p2}) + \beta A_0}
\]

\[
= \frac{A_0 \omega_{p1} \omega_{p2}}{s^2 + (\omega_{p1} + \omega_{p2})s + (1 + \beta A_0)\omega_{p1}\omega_{p2}}
\]

\[
p_{1,2} = \frac{-(\omega_{p1} + \omega_{p2}) \pm \sqrt{(\omega_{p1} + \omega_{p2})^2 - 4(1 + \beta A_0)\omega_{p1}\omega_{p2}}}{2}
\]

For \( p_1 = p_2 = -\frac{\omega_{p1} + \omega_{p2}}{2} \)

\( (\omega_{p1} + \omega_{p2})^2 - 4(1 + \beta A_0)\omega_{p1}\omega_{p2} = 0 \)

\( \Rightarrow \beta_1 = \frac{1}{A_0} \frac{(\omega_{p1} - \omega_{p2})^2}{4\omega_{p1}\omega_{p2}} \)

\( \Rightarrow \) still unconditional stable
Stability (cont.)

- Three-pole system

- Additional poles (and zeros) impact the phase to a much greater extend than they do the magnitude.

- If the feedback factor decreases, the circuit becomes more stable because the gain crossover move toward the origin while the phase crossover remains constant.
Stability (cont.)

Phase Margin

System is stable, if
\[ |L(j\omega_{-180^\circ})| < 1 \]
\[ \angle L(j\omega_{0_{dB}}) > -180^\circ \]

Phase Margin (PM) = \[ \angle L(j\omega_{0_{dB}}) + 180^\circ \]
Gain Margin (PM) = \[ -20 \log |L(j\omega_{-180^\circ})| \]

\[ \angle L(j\omega_{0_{dB}}) = -175^\circ \]
\[ \Rightarrow \beta H(j\omega_{0_{dB}}) = \exp(-j175^\circ) \]

Phase Margin (PM) = \[ \angle L(j\omega_{0_{dB}}) + 180^\circ = 5^\circ \]

\[ \frac{Y}{X}(j\omega_{0_{dB}}) = \frac{H(j\omega_{0_{dB}})}{1 + \beta H(j\omega_{0_{dB}})} = \frac{1/\beta}{1 + 1/L(j\omega_{0_{dB}})} \]
\[ = \frac{1/\beta}{1 + \exp(j175^\circ)} \]

\[ |\frac{Y}{X}(j\omega_{0_{dB}})| = \frac{11.5}{\beta} \Rightarrow \text{large peaking} \]
Stability (cont.)

- 45° phase margin

\[
\angle L(j \omega_{0_{dB}}) = -135^\circ \quad \Rightarrow \beta H(j \omega_{0_{dB}}) = \exp(-j135^\circ)
\]

Phase Margin (PM) = \(\angle L(j \omega_{0_{dB}}) + 180^\circ = 45^\circ\)

\[
\frac{Y}{X}(j \omega_{0_{dB}}) = \frac{1/\beta}{1 + \exp(j135^\circ)} = \frac{1/\beta}{0.293 + j0.707}
\]

\[
\left|\frac{Y}{X}(j \omega_{0_{dB}})\right| = \frac{1.3}{\beta} \quad \Rightarrow 30\% \text{ peak}
\]
Stability (cont.)

- Closed-loop time response for various phase margin

- $PM = 60^\circ, \quad \left| \frac{Y}{X}(j\omega_{db}) \right| = \frac{1}{\beta} \Rightarrow$ negligible frequency peaking
  $\Rightarrow$ little ringing and fast settling

- Example: unity-gain buffer (large-signal step response)

  $(W/L)=50 \ \mu m / 0.6 \mu m$
  $f_i=150 \ MHz$
  $PM=65^\circ$
  Nonlinearity of the circuit causes the variation of the poles and zeros during transient.
Practical Design Parameters

\[ V_{out} = A_v(s)(v_d + V_{OS}) + A_{cm}(s)v_{cm} + A_{dd}(s)v_{dd} + A_{ss}(s)v_{ss} \]

- Gain and bandwidth (gain-bandwidth product)
- Phase margin
- Slew rate and settling time
- Offset voltage
- Common-mode range (CMR)
- Common-mode rejection ratio (CMRR) \[ CMRR = \left| \frac{A_v}{A_{cm}} \right| \]
- Power-supply rejection ratio (PSRR)

\[ PSRR^+ = \left| \frac{A_v}{A_{dd}} \right| \]
\[ PSRR^- = \left| \frac{A_v}{A_{ss}} \right| \]
Practical Design Parameters (cont.)

Linear Settling Time

due to the finite unity-gain frequency of the opamp

![Diagram of linear settling time](image)

\[ A(s) = \frac{A_0}{1 + s/\omega_{p1}} \quad \text{(Note: } \omega_t \approx A_0 \omega_{p1}) \]

For \( \omega_{p1} \ll \omega \ll \omega_t \), \( A(s) \approx \frac{\omega_t}{s} \).

Closed-loop gain:

\[ A_{CL}(s) = \frac{A(s)}{1 + \beta A(s)} \approx \frac{1}{\beta} \frac{1}{1 + s/\beta \omega_t} \]

\[ A_{CL0} \approx \frac{1}{\beta} \quad \text{and} \quad \omega_{3dB} = \frac{1}{\tau} \approx \beta \omega_t \]

Step Response:

\[ v_{in}(t) = V_{step} u(t) \quad \Rightarrow \quad V_{in}(s) = \frac{V_{step}}{s} \]

\[ v_{out}(t) = V_{step} (1 - e^{-t/\tau}) \]

- 1% accuracy \( \Rightarrow 4.6\tau \)
- 0.1% accuracy \( \Rightarrow 6.9\tau \)

**Slope**:

\[ \text{Slope} = \lim_{t \to 0} \frac{dV_{out}}{dt} = \frac{V_{step}}{\tau} \]

If \( SR > \text{Slope} \), no slew-rate limiting occurs.
Example: Opamp Gain and Unity Gain Frequency for an ADC

\[ A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} \]

\[ = \frac{1}{\beta \left(1 + \frac{1}{A_{OL}}\right)} \]

\[ \approx \frac{1}{\beta} \left(1 - \frac{1}{\beta A_{OL}}\right) \]

\[ \frac{1}{\beta A_{OL}} < \frac{1}{2^{N+1}} \quad (0.5\text{LSB}) \]

\[ A_{OL} > 2^{N+1} \frac{\beta}{\beta} \]

\[ v_{out} = V_{out,\text{final}} \left(1 - e^{-t/\tau}\right) \]

\[ \tau = \frac{1}{\omega_{-3dB}} = \frac{1}{\beta \omega_{i}} \]

\[ (\omega_{i} : \text{unity - gain frequency of opamp}) \]

To settle within \( \frac{\Delta}{2} \), \( e^{-t_{\text{settle}}/\tau} < \frac{1}{2^{N+1}} \)

\[ t_{\text{settle}} < \tau \cdot \ln 2^{N+1} = \frac{\ln 2^{N+1}}{\beta \omega_{i}} \]

\[ f_{i} > \frac{\ln 2^{N+1}}{2\pi \beta \cdot t_{\text{settle}}} = 0.11(N + 1) \]

\[ \beta = \frac{C_{F}}{C_{I} + C_{F}} \]

For \( C_{I} = C_{F} \), \( \beta = 0.5 \)

\[ N = 12 \quad \Rightarrow A_{v} > 2^{N+2} = 2^{14} \, V/V \quad (84\text{dB}) \]

If \( t_{\text{settle}} = \frac{1}{2f_{CLK}} \), \( f_{i} > \frac{0.11(N + 1)}{\beta \cdot t_{\text{settle}}} = 0.44(N + 1)f_{CLK} \)

\[ f_{CLK} = 100\text{MHz} \quad \Rightarrow f_{i} = 572\text{MHz} \]
**Telescopic Opamp**

### Design Equations

Let \( I_{D9} = \alpha I_B \) \( \Rightarrow P = V_{DD}(1 + \alpha)I_B \) \( \Rightarrow I_{D1,2} = \frac{I_{D9}}{2} = \frac{\alpha P}{2V_{DD}(1 + \alpha)} \)

\[ R_{out} \approx \left( g_{m4}r_{ds4}r_{ds2} \right) \left| \left( g_{m6}r_{ds6}r_{ds8} \right) \right| = \frac{2}{(\lambda_p^2 V_{EB4} + \lambda_n^2 V_{EB6})I_{D1}} = \frac{4V_{DD}(1 + \alpha)}{\alpha P(\lambda_p^2 V_{EB4} + \lambda_n^2 V_{EB6})} \]

\[ A_v = g_{m1}R_{out} = \frac{4I_{D1}/V_{EB1}}{(\lambda_p^2 V_{EB4} + \lambda_n^2 V_{EB6})I_{D1}} = \frac{4}{(\lambda_p^2 V_{EB4} + \lambda_n^2 V_{EB6})V_{EB1}} \]

\[ \omega_{p1} = \frac{1}{R_{out}C_L} \]

\[ GB = \omega_t \approx A_v \times \omega_{p1} = \frac{g_{m1}C_L}{\omega_1} = \frac{\mu_n C_{ox} \left( \frac{W}{L} \right) V_{EB1}}{C_L} = \frac{2I_{D1}}{V_{EB1}C_L} = \frac{\alpha P}{V_{DD}(1 + \alpha)V_{EB1}C_L} \]

\[ PM \approx 180 - \tan^{-1} \left( \frac{\omega_t}{\omega_{p1}} \right) \]

\[ SR = \frac{I_{D9}}{C_L} = V_{EB1}GB \]

\[ V_{out(max)} = V_{DD} - V_{EB9} - V_{EB1} - V_{EB3} \]

\[ V_{out(min)} = V_{EB5} + V_{EB7} \]
Folded-Cascode Opamp

Design Equations

- consuming more power
- wider ICMR
- slightly larger output swing

\[ R_{\text{out}} \approx \left[ g_{m6}r_{ds6}(r_{ds1} \parallel r_{ds3}) \parallel (g_{m8}r_{ds8}r_{ds10}) \right] \]

\[ A_{v0} \approx g_{m1}R_{\text{out}} \]

\[ \omega_{-3dB} \approx \frac{1}{R_{\text{out}}C_L} \]

\[ CMR+ = V_{DD} - V_{eff3} + V_{m1} \quad CMR- = V_{eff8} + V_{GS1} \]

Output swing: \[ V_{DD} - V_{eff3} - V_{eff6} \sim V_{eff8} + V_{eff10} \]
Folded-Cascode Opamp (cont.)

✿ Bias Currents and Slew Rate

\[ I_{bias1} > \frac{I_{bias2}}{2} \]

\[ I_{bias1} > I_{bias2} / 2 \]

\[ I_{bias1} - I_{bias2} \]

\[ Q_{bias1} \]

Case 1

\[ I_{bias1} \leq I_{bias2} < 2I_{bias1} \]

\[ SR = \frac{I_{bias1}}{C_L} \]

\[ I_{bias2} \leq I_{bias1} \]

\[ SR = \frac{I_{bias1} - (I_{bias1} - I_{bias2})}{C_L} = \frac{I_{bias2}}{C_L} \]
Folded-Cascode Opamp (cont.)

- Purposes for $Q_{11}$ and $Q_{12}$
  - $Q_{11}$ and $Q_{12}$ are turned off during normal operation and almost have no effect on the opamp.
  - $Q_{11}$ and $Q_{12}$ act as clamp transistors to prevent the drain voltages $Q_1$ and $Q_2$ from having large transients where they change from their small-signal voltages to voltages very close to the negative power-supply voltage. Thus, the opamp can recover more quickly following a slew-rate condition.
  - Increase the slew-rate performance of the opamp:
    \[
    I_{bias1} \leq I_{bias2} < 2I_{bias1}
    \]
    \[
    SR = \frac{I_{bias2}}{C_L}
    \]
Folded-Cascode Opamp (cont.)

Design Example

\[ A_{vo} = \frac{4}{V_{EB1}[\alpha_\lambda_p^2 V_{EB5} + \lambda_n (\lambda_n + \kappa_p + \alpha \lambda_n)V_{EB1}]} \]

\[ GB = \frac{P}{(1 + \alpha)V_{EB1} V_{DD} C_L} \]

Specification:

<table>
<thead>
<tr>
<th>Avo (dB)</th>
<th>GB (MHz)</th>
<th>P (mW)</th>
<th>( \alpha )</th>
</tr>
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</table>

Set VEB to calculate the performance.

VEB1  VEB5  VBE7  VEB3  VBE9  VEB11

Calculation Results:

<table>
<thead>
<tr>
<th>Avo (dB)</th>
<th>GB (MHz)</th>
<th>IB (( \mu A ))</th>
<th>SR (V/( \mu s ))</th>
<th>CMR+</th>
<th>CMR-</th>
<th>Vomax</th>
<th>Vomin</th>
<th>Rout (M( \Omega ))</th>
</tr>
</thead>
<tbody>
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</table>

M1  M5  M7

ID (\( \mu A \))

W/L
Gain Boosting

- Increasing the Output Impedance by Feedback

\[ R_{\text{out}} \approx g_m r_o^2 r_{o1} \]

- Gain Boosting in Cascode Stage

\[ R_{\text{out}} \approx (g_m r_o^3) g_m^2 r_{o2}^2 r_{o1} \]

\[ A_v = -g_m R_{\text{out}} \approx -g_m g_m^3 r_o^3 g_m^2 r_{o2}^2 r_{o1} \]

\[ V_{\text{out(min)}} = V_{GS3} + V_{eff/2} \]
Gain Boosting (cont.)

Gain Boosting for Differential Cascode Stage

\[ V_{out\,(min)} = V_{ss2} + V_{GS5} + V_{eff\,3} \]
Gain Boosting (cont.)

Folded-Cascode Circuit Used as Auxiliary Amplifier

\[ V_{X,Y(\text{min})} = V_{\text{ISS1}} + V_{\text{eff1}} \]
\[ V_{\text{out(min)}} = V_{\text{ISS1}} + V_{\text{eff1}} + V_{\text{eff3}} \]

\[ A_1 = g_{m2} R_{\text{out1}} \]
\[ R_{\text{out1}} \approx \left[ g_{m7} r_{o7} \left( r_{o5} \parallel r_{o9} \right) \right] / \left( g_{m11} r_{o11} r_{o13} \right) \]
\[ R_{\text{out}} \approx (g_{m5} R_{\text{out1}}) g_{m3} r_{o3} r_{o1} \]
\[ A_y = -g_{m1} R_{\text{out}} \approx -g_{m1} g_{m3} r_{o3} g_{m2} r_{o2} r_{o1} \]
Gain Boosting (cont.)

Gain Boosting Applying to Signal and Load Paths

- In contrast to two-stage opamps, where the entire signal experiences the poles associated with each stage, in a gain-boosted opamp, most of the signal directly flows through the cascode devices to the output. Only a small error component is processed by the gain-boosting amplifier and slowed down.
Fully-Differential Opamps

The Need for Common-Mode Feedback Circuits

The input and output common-mode levels are well defined, equal to $V_{DD} - I_{SS}R_D / 2$.

The input and output common-mode levels are not well defined. Mismatches between the currents in PMOS and NMOS transistors may result in large output voltage changes.

$V_{out} = (I_P - I_N)(R_P // R_N)$
Continuous-Time CMFB Circuits

- Common-Mode Feedback (CMFB) Circuits

- Common-mode feedback with resistive sensing
Continuous-Time CMFB Circuits (cont.)

- **Common-mode feedback using source followers**
  - Note: $R_1$ and $R_2$ or $I_1$ and $I_2$ must be large enough to ensure that $M_7$ or $M_8$ is not starved at a large output swing.

- **Sensing and controlling output CM level**
SC CMFB Circuits

Switched-capacitor CMFB circuit

- more accurately defined CM level

Reset mode: $S_1$ on $\Rightarrow V_{CM} = V_{GS6,7} + V_{GS5}$

$V_{C1,C2} = V_{GS6,7}$

Amplification mode: $S_1$ off

Reset mode: $S_{1,4,5}$ on $\Rightarrow V_{C1,C2} = V_{CM} - V_{GS6}$

Amplification mode: $S_{4,5}$ on $\Rightarrow V_{out} = V_{C1,C2} + V_{GS5} \approx V_{CM}$
### SC CMFB Circuits (cont.)

#### Another example

\[ \dot{\phi}_1 : \]
\[ Q_1^+ = C_C (V_{out}^+ - V_{ctrl1}) + C_S (V_{cm} - V_{bias}) \]
\[ Q_1^- = C_C (V_{out}^- - V_{ctrl1}) + C_S (V_{cm} - V_{bias}) \]

\[ \dot{\phi}_2 : \]
\[ Q_2^+ = (C_C + C_S) (V_{out}^+ - V_{ctrl2}) \]
\[ Q_2^- = (C_C + C_S) (V_{out}^- - V_{ctrl2}) \]

\[ \Rightarrow \Delta Q^+ + \Delta Q^- = 0 \]
\[ \Rightarrow (Q_2^+ - Q_1^+) + (Q_2^- - Q_1^-) = 0 \]
\[ \Rightarrow 2(C_C + C_S)(V_{out,cm} - V_{ctrl2}) = 2C_C (V_{out,cm} - V_{ctrl1}) + 2C_S (V_{cm} - V_{bias}) \]

\[ \Rightarrow V_{ctrl2} = \frac{C_C}{C_C + C_S} V_{ctrl1} + \frac{C_S}{C_C + C_S} (V_{out,cm} - V_{cm} + V_{bias}) \]

For \( V_{ctrl2} = V_{ctrl1} \), \( V_{out,cm} = V_{cm} - (V_{bias} - V_{ctrl1}) \)
Two-Stage Opamps

- Two-Stage CMOS Opamp with Output Buffer

- Equivalent Circuit for Uncompensated Opamp (without Cc and M₁₆)

\[ g_{mI} = g_{m1} \quad R_I = r_{ds2} // r_{ds4} \]

\[ g_{mII} = g_{m7} \quad R_{II} = r_{ds6} // r_{ds7} \]
Two-Stage Opamps (cont.)

- DC gain:
  \[ A_{v1} = -g_{m1} R_I \]
  \[ A_{v2} = -g_{mII} R_{II} \]
  \[ A_{v3} \approx g_{m8} / (G_L + g_{m8}) \]
  \[ A_{vo} = A_{v1} \times A_{v2} \times A_{v3} \]

**Frequency Response**

- Without Compensation

\[
\omega_{p1}' = \frac{1}{R_I C_I} \quad \omega_{p2}' = \frac{1}{R_{II} C_{II}}
\]

\[
A_v(s) = \frac{A_{vo}}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}
\]

\[
|A_v(j\omega)| = \frac{A_{vo}}{\sqrt{[1 + \left(\frac{\omega}{\omega_{p1}}\right)^2][1 + \left(\frac{\omega}{\omega_{p2}}\right)^2]}}
\]

\[
\angle A_v(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p2}}\right)
\]

- Due to the square-law nature, \(\omega_{p1}\) and \(\omega_{p2}\) are usually quite close to each other.
  - \(\Rightarrow\) Phase margin is significantly less than 45°.
  - \(\Rightarrow\) The opamp must be compensated before used in a closed-loop configuration.
**Compensation**

- **With Compensation Capacitor (Cc)**

\[ \omega_{p1} \approx \frac{1}{R_l[(1 - A_{v2})C_C + C_I]} \approx \frac{1}{R_l(g_{mll}R_{II}C_C)} \]

\[ \omega_{p2} \approx \frac{g_{mll}C_C}{C_I C_{II} + C_{II} C_C + C_I C_C} \]

\[ \omega_z = \frac{g_{mll}}{C_C} \quad \text{(RHP zero)} \]

\[ A_v(s) = \frac{A_v(1 - \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \]

\[ \angle A_v(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p2}}\right) \]

Translating the dominant pole toward origin to improve stability

Pole splitting as a result of Miller compensation
Compensation (cont.)

- Unity-gain frequency and gain-bandwidth product

\[ \omega_t = \frac{\omega_m \omega_{p1}}{C C} \quad \text{(gain - bandwidth product)} \]

- Effect of RHP zero

Find unity - gain frequency.

Since \( \omega_s \gg \omega_{p1} \), \( A_v(s) \approx \frac{A_v}{s} \quad \Rightarrow \quad A_v(j \omega_s) = \left| \frac{A_v \omega_{p1}}{\omega_s} \right| = 1 \)

\[ \Rightarrow \omega_t = \frac{\omega_m \omega_{p1}}{C C} \quad \text{(gain - bandwidth product)} \]
Compensation (cont.)

Effect for the output stage

Find zero by setting $v_o = 0$.

$\Rightarrow g_{m9}v_{o1} = g_{m8}v_{o2}$

Using node equation at $v_{o2}$, one can obtain

$$(g_{mll} - sC_C)v_{o1} + [s(C_C + C_{ll}) + \frac{1}{R_{ll}}]v_{o2} = 0$$

$\Rightarrow (g_{mll} - sC_C)\frac{g_{m8}}{g_{m9}} + [s(C_C + C_{ll}) + \frac{1}{R_{ll}}] = 0$

$\Rightarrow s[(1 - \frac{g_{m8}}{g_{m9}})C_C + C_{ll}] + g_{mll}\frac{g_{m8}}{g_{m9}} + \frac{1}{R_{ll}} = 0$  $\Rightarrow s_z = -\frac{g_{mll}\frac{g_{m8}}{g_{m9}} + \frac{1}{R_{ll}}}{(1 - \frac{g_{m8}}{g_{m9}})C_C + C_{ll}}$

For $g_{m8} = g_{m9}$,

$$s_z = -\frac{g_{mll} + \frac{1}{R_{ll}}}{C_{ll}} \approx -\frac{g_{mll}}{C_{ll}} \quad \text{(LHP zero)}$$
Lead Compensation (Rz)

Several ways to choose $R_z$:
- Taking $R_z = 1/g_{mII}$, one can eliminate the RHP zero.
- Let $\omega_z = \omega_{p2}$ to cancel the nondominant pole.
  However, $\omega_{p2}$ is often not known a priori.
- Let $\omega_z = 1.2\omega_i$ to increase the phase margin.

\[
\begin{align*}
\omega_{p1} & \approx \frac{1}{R_i[(1-A_{v2})C_c + C_I]} \approx \frac{1}{R_i(g_{mlt}R_{II}C_c)} \\
\omega_{p2} & \approx \frac{g_{mlt}C_c}{C_IC_{II} + C_{II}C_I + C_IC_C} \\
\omega_{p3} & = \frac{1}{R_zC_I} \\
\omega_z & = \frac{1}{\left(\frac{1}{g_{ml}}-R_z\right)C_c} \\
\omega_i & \approx A_{v0}\omega_{p1} \approx \frac{g_{ml}}{C_c} \quad \text{(unity - gain frequency)}
\end{align*}
\]
Compensation (cont.)

- Other approaches to Remove RHP zero
  - Eliminating forward signal feedthrough
Compensation (cont.)

- **Indirect Current Feedback**

\[ \omega_z = \frac{g_{mcg}}{C_c} \quad \text{(LHP zero)} \]

\[
v_{out} = v_2
\]
Compensation (cont.)

- Indirect feedback compensation without additional power dissipation

Figure 24.24: The large-signal (500 mV to 900 mV) performance of the op-amp in Fig. 24.21 with $C_p = 0.24$ pF driving a 1 pF load. The low-to-high settling time is roughly 10 ns, while the high-to-low settling time, which is slew-rate limited, is roughly 60 ns. Note the different time scale when compared to Fig. 24.23.
Design Equations

- Slew rate
  \[ \frac{\Delta V}{\Delta t} = \frac{I_{D3}}{g_{m7}} \]

- First-stage gain
  \[ A_{V1} = -g_{m1} (r_{ds2} \parallel r_{ds4}) = -\frac{2g_{m1}}{I_{D3}(\lambda_2 + \lambda_4)} \]

- Second-stage gain
  \[ A_{G2} = -\frac{\Delta g_{m2} \Delta g_{m2} \Delta g_{m2} \Delta g_{m7}}{\Delta g_{m7} + \Delta \lambda_0} \]

- Gain-bandwidth
  \[ \omega_G = \frac{\Delta g_{m1}}{\Delta \lambda_0} \]

- First pole
  \[ \omega_{\lambda 0} \approx \frac{\Delta g_{m2} \Delta g_{m2} \Delta g_{m2} \Delta g_{m7}}{\Delta g_{m7} + \Delta \lambda_0} \]

- Second pole
  \[ \omega_{\lambda 0} \approx \frac{\Delta g_{m2} \Delta g_{m2} \Delta g_{m2} \Delta g_{m7}}{\Delta g_{m7} + \Delta \lambda_0} \]

- Zero \((R_C = 1/g_{m7})\)
  \[ \omega_z = \frac{1}{(\frac{1}{g_{m7}} - R_Z)C_C} \]

- Positive CMR
  \[ V_{cm(max)} = V_{DD} - V_{SD5(sat)} - V_{SG1} \]

- Negative CMR
  \[ V_{cm(min)} = V_{SS} + V_{GS3} + V_{Tp} \]

- Positive output swing
  \[ V_{out(max)} = V_{DD} - V_{SD6(sat)} - V_{GS8} \]

- Negative output swing
  \[ V_{out(min)} = V_{SS} + V_{DS9(sat)} \]

- Power dissipation
  \[ P_{diss} = (I_{D5} + I_{D6} + I_{D8} + I_{D10} + I_{D11})(V_{DD} - V_{SS}) \]

---

<table>
<thead>
<tr>
<th>( I_{D5} )</th>
<th>( I_{D6} )</th>
<th>( (W/L)_{1,2} )</th>
<th>( L_{1,2} )</th>
<th>( W_{3,4} )</th>
<th>( L_{3,4} )</th>
<th>( (W/L)_6 )</th>
<th>( W_7 )</th>
<th>( L_7 )</th>
<th>( C_C )</th>
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<tbody>
<tr>
<td>( A_V ) \uparrow</td>
<td>( (\downarrow)^{1/2} )</td>
<td>( (\downarrow)^{1/2} )</td>
<td>( (\uparrow)^{1/2} )</td>
<td>( \uparrow )</td>
<td>( \uparrow )</td>
<td>( (\uparrow)^{1/2} )</td>
<td>( \uparrow )</td>
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<td></td>
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<tr>
<td>( \omega_{\lambda 0} ) \uparrow</td>
<td>( (\uparrow)^{1/2} )</td>
<td>( (\uparrow)^{1/2} )</td>
<td>( \uparrow )</td>
<td>( \uparrow )</td>
<td>( \downarrow )</td>
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<tr>
<td>RHP Zero ( \uparrow )</td>
<td>( (\uparrow)^{1/2} )</td>
<td>( (\uparrow)^{1/2} )</td>
<td>( \uparrow )</td>
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</tr>
<tr>
<td>SR ( \uparrow )</td>
<td>( \uparrow )</td>
<td>( \downarrow )</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CL( \uparrow )</td>
<td>( \uparrow )</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Nonlinear Settling Time: due to slew-rate limiting

- Slew Rate: the maximum rate that output can change

\[
SR = \frac{dV_{\text{out}}}{dt}_{\text{max}} \\
\approx \frac{dV_C}{dt} = \frac{I_{C\text{max}}}{C_C} = \frac{I_{D5}}{C_C} = \frac{2I_{D1}}{C_C}
\]

Since \( C_C = \frac{g_{m1}}{\omega_0} \) and \( g_{m1} = \sqrt{2\mu_p C_{OX} \left( \frac{W}{L} \right)_1 I_{D1}} \),

\[ SR = (V_{SG1} + V_{qs})\omega_t = V_{\text{eff}}\omega_t \]

Slope = \[ \frac{dV_{\text{out}}}{dt} \bigg|_{t=0} = \frac{V_{\text{step}}}{\tau} \]

If \( SR > \text{Slope} \), no slew-rate limiting occurs.

Offset Voltage

- Random offset: due to device mismatches resulting from process variations. ⇒ employing matching layout technique

- Systematic offset: due to design error

For \( V_{in}^+ = V_{in}^- \),

\[ I_{D1} = I_{D2} = I_{D5} / 2. \]

Since \( V_{GS3} = V_{GS4}, V_{DS3} = V_{DS4} = V_{GS7} = V_{GS3} \).

⇒ M3 and M7 is equivalent to a current mirror.

\[ \frac{I_{D3}}{(W/L)_3} = \frac{I_{D7}}{(W/L)_7} \]

Also for the current mirror (M5 and M6),

\[ \frac{I_{D5}}{(W/L)_5} = \frac{I_{D6}}{(W/L)_6} \]

and \( I_{D6} = I_{D7} \)

\[ \frac{(W/L)_7}{(W/L)_4} = 2 \frac{(W/L)_6}{(W/L)_5} \]
Alternate Design Equations

Let \( I_{D6} = \alpha_1 I_{D5} \) and \( I_{D9} = \alpha_2 I_{D5} \). \( \Rightarrow P = V_{DD}(1 + \alpha_1 + \alpha_2)I_{D5} \)

\[
R_1 = r_{ds3} // r_{ds4} = \frac{1}{(\lambda_n + \lambda_p)I_{D1}} \quad \text{and} \quad R_2 = r_{ds6} // r_{ds7} = \frac{1}{(\lambda_n + \lambda_p)I_{D7}}
\]

\[
R_{out} = \frac{1}{g_{m8} + g_{ds8} + g_{ds9}} = \frac{1}{2I_{D9}/V_{EB8} + (\lambda_n + \lambda_p)I_{D9}}
\]

\[
= \frac{1}{I_{D9}(2/V_{EB8} + \lambda_n + \lambda_p)} = \frac{V_{DD}(1 + \alpha_1 + \alpha_2)}{2I_{D9}V_{EB8} + (\lambda_n + \lambda_p)}
\]

\[
A_{v1} = -g_{m1}R_1 = \frac{\mu_n C_{ox}(\frac{W}{L})_1 V_{EB1}}{(\lambda_n + \lambda_p)(\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_1 V_{EB1})} = \frac{2}{(\lambda_n + \lambda_p)V_{EB1}}
\]

\[
A_{v2} = -g_{m7}R_2 = \frac{2}{(\lambda_n + \lambda_p)V_{EB7}}
\]

\[
A_{v3} = g_{m8}R_{out} = \frac{\mu_n C_{ox}(\frac{W}{L})_8 V_{EB8}}{\mu_n C_{ox}(\frac{W}{L})_8 V_{EB8} + (\lambda_n + \lambda_p)(\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_8 V_{EB8})}
\]

\[
= \frac{1}{1 + (\lambda_n + \lambda_p)V_{EB8}}
\]

\[
A_{vo} = A_{v1} \times A_{v2} \times A_{v3} = \frac{4}{[(\lambda_n + \lambda_p)^2 V_{EB1} V_{EB7}][1 + (\lambda_n + \lambda_p)V_{EB8}]}\]

\[
\omega_1 \approx \frac{g_{m1}}{C_L} = \frac{\mu_n C_{ox}(\frac{W}{L})_1 V_{EB1}}{C_L}
\]

\[
= \frac{2I_{D1}}{V_{EB1}C_L} = \frac{P}{V_{DD}(1 + \alpha_1 + \alpha_2)V_{EB1}C_L}
\]

\[
\omega_2 \approx \frac{g_{m7}}{C_i + C_{II}} \approx \frac{g_{m7}}{C_{gs8}}
\]

\[
\omega_3 = 1.2\omega_1 \quad \Rightarrow g_{m7} = 1.2(1-x)g_{m1}
\]

\[
\omega_3 = \frac{1}{R_{out}C_I} \approx \frac{g_{m8}}{C_L} \quad (R_{out} \approx \frac{1}{g_{m8}})
\]

\[
PM \approx 90 - tan^{-1}\left(\frac{\omega_1}{\omega_2}\right) - tan^{-1}\left(\frac{\omega_1}{\omega_z}\right) - tan^{-1}\left(\frac{\omega_1}{\omega_3}\right)
\]

\[
SR = \frac{I_{D5}}{C_L} = V_{EB1}GB
\]
## Comparison

<table>
<thead>
<tr>
<th></th>
<th>Gain</th>
<th>Output Swing</th>
<th>Speed</th>
<th>Power Dissipation</th>
<th>Noise</th>
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<tbody>
<tr>
<td>Telescopic</td>
<td>Medium</td>
<td>Medium</td>
<td>Highest</td>
<td>Low</td>
<td>Low</td>
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<tr>
<td>Folded-Cascade</td>
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<td>Medium</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
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<tr>
<td>Two-Stage</td>
<td>High</td>
<td>Highest</td>
<td>Low</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>Gain-Boosted</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
<td>Medium</td>
</tr>
</tbody>
</table>
Cascode-Cascade Opamp

\[ P = V_{DD} (1 + \alpha) I_B = 2V_{DD} (1 + \alpha) I_1 \]

\[ A_{vo} = \frac{g_{m1}}{g_{o3} g_{o1} / g_{m3} + g_{o5} g_{o5} / g_{m5} + g_{o9} + g_{o11}} \]

\[ = \frac{2I_1}{V_{EB1} \lambda_1 \lambda_2 I_1^2 / (2I_1 / V_{EB3}) + \lambda_5 \lambda_7 I_1^2 / (2I_1 / V_{EB5}) V_{EB9} \lambda_9 I_{11} + \lambda_1 I_{11}} \]

\[ = \frac{8}{V_{EB1} (\lambda_1 \lambda_3 V_{EB3} + \lambda_5 \lambda_7 V_{EB5} V_{EB9} (\lambda_9 + \lambda_{11}) = \frac{211}{8} (\lambda_2^2 V_{EB3} + \lambda_3^2 V_{EB5}) V_{EB9} (\lambda_9 + \lambda_{11}} \]

\[ GB = \frac{g_{m1}}{C_C V_{EB1} C_C} = \frac{2I_1}{V_{EB1} (1 + \alpha) C_C V_{EB1}} \]

\[ \omega_{p1} = -\frac{GB}{A_{vo}} = -\frac{P(\lambda_1 \lambda_3 V_{EB3} + \lambda_5 \lambda_7 V_{EB5} V_{EB9} (\lambda_9 + \lambda_{11})}{8V_{DD} (1 + \alpha) C_C} \]

\[ \omega_{p2} \approx -\frac{g_{m9} C_C}{C_j C_L + C_L C_C + C_C C_I} \approx -\frac{g_{m9}}{C_L} \approx -\frac{\alpha I_B}{V_{EB9} C_L} = -\frac{\alpha P}{V_{DD} (1 + \alpha) C_j V_{EB9}} \]

\[ \omega_{p3} = -\frac{1}{R_z C_I} \]

\[ \omega_z = \frac{1 - R_Z) C_C}{g_{m9} \omega_{p2} C_L + R_Z C_C} = \frac{1}{C_C \omega_{p2} C_L + R_Z C_C} = \frac{1}{V_{DD} (1 + \alpha) V_{EB9} - R_Z C_C} \]

\[ SR = \frac{I_B}{C_C} = \frac{P}{V_{DD} (1 + \alpha) C_C} = GB \times V_{EB1} \]
Low-Voltage Opamp

- CMOS Technology
Low-Voltage Opamp (cont.)

- Input Common-Mode Range of a Differential Input Stage

\[
\begin{align*}
V_{DD(\text{min})} &= V_{SD3(sat)} - V_{m1} + V_{GS1} + V_{DS5(sat)} \\
&= V_{SD3(sat)} + V_{DS1(sat)} + V_{DS5(sat)} \\
V_{icm(\text{max})} &= V_{DD} - V_{SD3(sat)} + V_{tn1} \\
V_{icm(\text{min})} &= V_{GS1} + V_{DS5(sat)}
\end{align*}
\]

- For \( V_{\text{sat}} = 0.3V \), \( V_{DD(\text{min})} = 0.9V \)
- \( V_{DD} = 1.5V \) and \( V_{tn1} = 0.7V \),
  \[ V_{icm(\text{max})} = 1.9V \] and \( V_{icm(\text{min})} = 1.3V \)
Parallel NMOS and PMOS Differential Input Stage

\[
V_{on} = V_{DSN5(sat)} + V_{GSN1} \\
V_{onp} = V_{DD} - V_{SDP5(sat)} - V_{SGP1}
\]

- Effective input transconductance
Low-Voltage Opamp (cont.)

- Constant $g_m$ Differential Input Stage Using Current Compensation

\[ g_{mN} = \sqrt{2\mu_n C_{OX}} \left(\frac{W}{L}\right)_N I_n \]
\[ g_{mP} = \sqrt{2\mu_p C_{OX}} \left(\frac{W}{L}\right)_P I_p \]

Let $\beta = \mu_n C_{OX} \left(\frac{W}{L}\right)_N = \mu_p C_{OX} \left(\frac{W}{L}\right)_P$

\[ g_{mT} = \sqrt{2\beta} (\sqrt{I_n} + \sqrt{I_p}) \]

For $0 < V_{i_{cm}} < V_{o_{nn}}, I_p = 4I_b$.

For $V_{o_{nn}} < V_{i_{cm}} < V_{o_{np}}, I_n = I_p = I_b$.

For $V_{o_{np}} < V_{i_{cm}} < V_{DD}, I_n = 4I_b$. 

MOS Switches in Low-Voltage Design

- Pass Transistors

\[ R_e = \frac{V_{DS}}{I_D} \]

\[ R_p = \frac{1.5 - V_D}{I_D} \]

Note: Body of PMOS is tied to 1.5 V

---

Graphs showing the relationship between sweep, V, and V_{DS} for different W/L ratios.
MOS Switches in Low-Voltage Design (cont.)

- Problem for the switch

Use transmission gate.
  - Larger layout area
  - It may not turned on for low voltage.

Increase gate voltage to 2.3V.
MOS Switches in Low-Voltage Design (cont.)

- Charge Pumps (Voltage Generators)

![Diagram of Charge Pumps](image)

![Graph](image)
MOS Switches in Low-Voltage Design (cont.)

- Charge-Pump Clock Driver

- Nonoverlapping clock generation circuit
Bootstrap circuit and switching device.

Switched-Oppamp

- **Design concept**

  - Switched-capacitor integrator
  - Switchable opamp
  - Switched-capacitor biquad
  - Switched-opamp biquad
  - Input structure

Switched-Opamp

Example: Fully-Differential Switched-Opamp MDAC

Outline

- Analog and Mixed-Signal Design in the SOC Era
- Current Mirrors and Biasing Circuits
- Single-Stage Amplifiers
- Operational Amplifiers
- Layout of Analog and Mixed-Signal ICs
Layout Considerations

Differences Between Layout and Circuit

The differences are mainly due to the following reasons:

- Lateral diffusion
- Etching under the protection
- Boundary dependent etching
- Error in the pattern size due to Tri-dimensional effects

These effects are not very substantial for digital systems; but they may have a significant impact on the accuracy of analog circuits and must be avoided or compensated.
Layout Considerations (cont.)

Absolute and Relative Accuracy

<table>
<thead>
<tr>
<th>Silicide</th>
<th>Resistor Type</th>
<th>$R_s$ (ohms/sq) AVG.</th>
<th>TCR1 (ppm/C$^2$) AVG.</th>
<th>TCR2 (ppm/C$^3$) AVG.</th>
<th>VCR1 (ppm/V) AVG.</th>
<th>VCR2 (ppm/V$^2$) AVG.</th>
<th>Mismatch % ΔR/R</th>
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<tbody>
<tr>
<td>n-well</td>
<td>n+</td>
<td>500 ± 10</td>
<td>2400 ± 50</td>
<td>7 ± 0.5</td>
<td>8000 ±</td>
<td>500 ± 50</td>
<td>&lt; 0.1</td>
</tr>
<tr>
<td>n+w</td>
<td>p+</td>
<td>120 ± 1</td>
<td>21 ± 10</td>
<td>0.6 ± 0.03</td>
<td>700 ± 50</td>
<td>150 ± 15</td>
<td>&lt; 0.5</td>
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<tr>
<td>p+</td>
<td>n+ diff</td>
<td>300 ± 5</td>
<td>160 ± 10</td>
<td>0.8 ± 0.03</td>
<td>600 ± 50</td>
<td>150 ± 15</td>
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<tr>
<td>n+</td>
<td>p+ diff</td>
<td>100 ± 2</td>
<td>1500 ± 10</td>
<td>0.04 ± 0.1</td>
<td>2500 ± 50</td>
<td>350 ± 20</td>
<td>&lt; 0.4</td>
</tr>
<tr>
<td>p+</td>
<td>n+</td>
<td>125 ± 3</td>
<td>1400 ± 20</td>
<td>0.4 ± 0.1</td>
<td>80 ± 80</td>
<td>100 ± 25</td>
<td>&lt; 0.6</td>
</tr>
<tr>
<td>n+</td>
<td>p+</td>
<td>125 ± 3</td>
<td>1400 ± 20</td>
<td>0.4 ± 0.1</td>
<td>80 ± 80</td>
<td>100 ± 25</td>
<td>&lt; 0.6</td>
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<tr>
<td>p+</td>
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<td>3 ± 0.3</td>
<td>3300 ± 90</td>
<td>1.0 ± 0.2</td>
<td>2500 ± 125</td>
<td>3800 ± 400</td>
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<tr>
<td>p+</td>
<td>p+</td>
<td>2 ± 0.1</td>
<td>3600 ± 50</td>
<td>1.0 ± 0.2</td>
<td>2500 ± 400</td>
<td>5500 ± 250</td>
<td>&lt; 0.7</td>
</tr>
<tr>
<td>p+</td>
<td>n+ diff</td>
<td>3 ± 0.1</td>
<td>3700 ± 50</td>
<td>1.0 ± 0.2</td>
<td>350 ± 150</td>
<td>600 ± 60</td>
<td>&lt; 1.0</td>
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<tr>
<td>p+</td>
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<td>1.0 ± 0.2</td>
<td>150 ± 50</td>
<td>800 ± 40</td>
<td>&lt; 1.0</td>
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</tbody>
</table>
Layout Considerations (cont.)

- Layout of an analog MOS transistor
  - Poor layout and its equivalent circuit

- Correct Layout

Metal profile with multi-contacts and only one contact
Layout Considerations (cont.)

- Layout of a wide transistor
  - Poor layout
  - Correct layout (split into several parallel transistors)
Layout Considerations (cont.)

- Layout of Matching Transistors
  - Sources causing transistor mismatches
    - Gradient effect existing in the fabrication process
    - To minimize the effect, two transistors that must be matched to each other should be placed very close.
    - For wide transistors, layout techniques to improve matching must be employed.
Layout Considerations (cont.)

- MOS Matching Model

\[ \sigma^2(\Delta V_i) = \frac{A_{VT}^2}{WL} \]
\[ \frac{\sigma^2(\Delta \beta)}{\beta^2} = \frac{A_{\beta}^2}{WL} \]

![Graphs of NMOS and PMOS](image.png)

Fig. 1. Matching parameters \( A_{VT} \) and \( A_{\beta} \) from different technology nodes for (a) nMOS and (b) pMOS devices (see also Table I).
Errors in Matched MOS Transistor Pairs

\[
\frac{\sigma^2(\Delta I_{DS})}{I_{DS}^2} = \frac{\sigma^2(\Delta \beta)}{\beta^2} + \left(\frac{g_m}{I}\right)^2 \sigma^2(\Delta V_i)
\]

\[
\sigma^2(\Delta V_{GS}) = \sigma^2(\Delta V_i) + \frac{1}{(g_m / I)^2} \frac{\sigma^2(\Delta \beta)}{\beta^2}
\]

\[
\frac{\sigma^2(\Delta \beta)}{\beta^2} = \left(\frac{g_m}{I}\right)^2 \sigma^2(\Delta V_i) \quad \Rightarrow \quad \left(\frac{g_m}{I}\right)_m = \frac{A_\beta}{A_{VT}}
\]
### TABLE 1

**Matching Proportionality Constants for Size Dependence for Different Industrial CMOS Processes**

<table>
<thead>
<tr>
<th>Technology</th>
<th>Type</th>
<th>$A_{VT}$</th>
<th>$A_3$</th>
<th>$(g_m/I_{DS})_m$</th>
<th>$(V_{GS} - V_T)_m$</th>
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<td>2.5μm [18]</td>
<td>nMOS</td>
<td>30</td>
<td>2.3</td>
<td>0.77</td>
<td>2.61</td>
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<td></td>
<td>pMOS</td>
<td>35</td>
<td>3.2</td>
<td>0.91</td>
<td>2.19</td>
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<td>1.2μm [19]</td>
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<td>1.8</td>
<td>0.86</td>
<td>2.33</td>
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<td></td>
<td>pMOS</td>
<td>25</td>
<td>4.2</td>
<td>1.68</td>
<td>1.19</td>
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<td>1.0μm [15]</td>
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</table>
Layout Considerations (cont.)

- Layouts of a Differential Pair

- Normal layout
- Inter-digitized layout
- Common-centroid layout
Layout Considerations (cont.)

- Orientation of transistors
  - Poor layout of transistors with different orientation

- Boundary dependent etching

  Compensation of boundary dependent etching with dummy elements
Layout Considerations (cont.)

- Layout or Resistors

\[ R = 2R_{\text{cont}} + R_s \frac{L}{W} \]

- Layout of two matched resistors

\[ R_s : \text{sheet resistor (}\Omega/\text{sq}) \]
Layout Considerations (cont.)

- Resistance is temperature-dependent.
  Matched resistors should be arranged with their centroids placed symmetrical with respect to the power devices.

- Resistor realized by well diffusion
Layout Considerations (cont.)

Layout of Capacitors

- Cross-section and layout of a capacitor

\[
C = \frac{\varepsilon_{ox}}{t_{ox}} \times A \\
A = W \times L \\
P = 2(W + L)
\]

Undercut:

\[
A' = (W - 2x)(L - 2x) \\
\approx W \times L - 2x(W + L) \\
= A - xP
\]

⇒ Matching depends on the perimeter.
Layout Considerations (cont.)

- Layout of ratioed capacitors

  - Matched capacitor with common-centroid symmetry
  - Capacitors with non-integer multiple of unit capacitor
Layout of Analog Cells

- Use transistors with the same orientation.
- Minimize the source or the drain contact area by stacking transistors.
- Respect the symmetries that exist in the electrical network as well as in the layout to reduce offset.
- Use low resistive paths when a current needs to be carried.
- Shield critical nodes.

Example: two-stage Opamp

Placement of transistors in a stacked fashion
Layout Considerations (cont.)

- Corresponding layout

- Use of dummy transistors in the placement of transistors
Digital Noise Coupling

- Capacitive couplings
  - Analog lines routed parallel to the digital lines
  - Crossing between analog lines and clocks

Separation to reduce horizontal coupling
Dummy line for horizontal shielding
Layout Considerations (cont.)

- Coupling through the substrate
  - Using well-shielding

\[
\Delta V = R_1 I_{tot} + R_2 I_{analog} + L \frac{dI_{tot}}{dt}
\]

\[
I_{tot} = I_{analog} + I_{digital}
\]
Layout Considerations (cont.)

- Reduce $R_1$: keeping the digital and analog sections as separate as possible and merging them at the place very close to the supply pad.
- If possible, use separate pads for the analog and digital section.

When extra pins are available, separate pins for the analog and digital supply should be used.

Place the supply pins in the middle of the frames.

<table>
<thead>
<tr>
<th>Element</th>
<th>$C_{DIL}$</th>
<th>$H_{DIL}$</th>
<th>$C_{CC}$</th>
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<td>15 nH</td>
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</table>
Floor Planning of Mixed-Signal Blocks

- General guidelines
  - Put the analog critical components as far as possible from the digital elements.
  - Make the connections to the critical nodes as short as possible.
  - Avoid crossing between the analog biasing lines and digital busses.

- Path of bias and supply lines for basic analog cells

- Typical floorplan of an SC filter
Layout Considerations (cont.)

- Typical floorplan of a fully-differential SC filter

![Typical floorplan of a fully-differential SC filter](image)

- Typical floorplan of a mixed-signal chip

![Typical floorplan of a mixed-signal chip](image)
Layout Considerations (cont.)

- Block Diagram Layout of a Pipelined ADC
Layout Considerations (cont.)

- Decoupling Capacitors in a Mixed-Signal Chip

![Diagram of decoupling capacitors in a mixed-signal chip](image)

- On-chip decoupling capacitor for the digital circuitry.
References