Film Layers for an MSI Era NMOS Transistor

Figure 11.1
Process Flow in a Wafer Fab

Locations where thin films are deposited

Wafer fabrication (front-end)

Fig 11.2

Used with permission of Advanced Micro Devices

Semiconductor Manufacturing Technology
by Michael Quirk and Julian Serda

Figure 11.2
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Introduction

• Film Layering in Wafer Fab
  – Diffusion
  – Thin Films

• Film Layering Terminology

• Multilayer Metallization
  – Metal Layers
  – Dielectric Layers
Multilevel Metallization on a ULSI Wafer

Figure 11.3
Metal Layers in a Chip

Micrograph courtesy of Integrated Circuit Engineering

Photo 11.1
Film Deposition

Thin Film Characteristics

- Good step coverage
- Ability to fill high aspect ratio gaps (conformality)
- Good thickness uniformity
- High purity and density
- Controlled stoichiometries
- High degree of structural perfection with low film stress
- Good electrical properties
- Excellent adhesion to the substrate material and subsequent films
Solid Thin Film

Thin films are very thin in comparison to the substrate.
Film Coverage over Steps

Conformal step coverage

Nonconformal step coverage
Aspect Ratio for Film Deposition

Aspect Ratio = \frac{\text{Depth}}{\text{Width}}

\text{Aspect Ratio} = \frac{500 \text{ Å}}{250 \text{ Å}} = \frac{2}{1}

Figure 11.6
High Aspect Ratio Gap

Photograph courtesy of Integrated Circuit Engineering
Stages of Film Growth

- Gas molecules
- Nucleation
- Coalescence
- Continuous film

Substrate
## Techniques of Film Deposition

<table>
<thead>
<tr>
<th>Chemical Processes</th>
<th>Physical Processes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Chemical Vapor Deposition (CVD)</strong></td>
<td><strong>Physical Vapor Deposition</strong></td>
</tr>
<tr>
<td>Atmospheric Pressure CVD (APCVD) or Sub-Atmospheric CVD (SACVD)</td>
<td>Electrochemical deposition (ECD), commonly referred to as electroplating</td>
</tr>
<tr>
<td>Low Pressure CVD (LPCVD)</td>
<td>Electroless Plating</td>
</tr>
<tr>
<td>Plasma Assisted CVD:</td>
<td></td>
</tr>
<tr>
<td>Plasma Enhanced CVD (PECVD)</td>
<td></td>
</tr>
<tr>
<td>High Density Plasma CVD (HDPCVD)</td>
<td></td>
</tr>
<tr>
<td>Vapor Phase Epitaxy (VPE) and Metal-organic CVD (MOCVD)</td>
<td></td>
</tr>
<tr>
<td>Dielectrics: Chapter 11</td>
<td>Chapter 12</td>
</tr>
<tr>
<td>Metals: Chapter 12</td>
<td></td>
</tr>
</tbody>
</table>
Chemical Vapor Deposition

The Essential Aspects of CVD

1. Chemical action is involved, either through chemical reaction or by thermal decomposition (referred to as pyrolysis).

2. All material for the thin film is supplied by an external source.

3. The reactants in a CVD process must start out in the vapor phase (as a gas).
Chemical Vapor Deposition Tool

Photograph courtesy of Novellus, Sequel CVD
CVD Reaction

- CVD Reaction Steps
- Rate Limiting Step
- CVD Gas Flow Dynamics
- Pressure in CVD
- Doping During CVD
  - PSG
  - BSG
  - FSG
Schematic of CVD Transport and Reaction Steps

1) Mass transport of reactants
2) Film precursor reactions
3) Diffusion of gas molecules
4) Adsorption of precursors
5) Precursor diffusion into substrate
6) Surface reactions
7) Desorption of byproducts
8) By-product removal

Gas delivery → CVD Reactor → Continuous film
Substrate

Figure 11.8
Gas Flow in CVD

Figure 11.9
Figure 11.10

Boundary Layer at Wafer Surface

- Continuous gas flow
- Diffusion of reactants
- Boundary layer
- Deposited film
- Silicon substrate
CVD Deposition Systems

- CVD Equipment Design
  - CVD reactor heating
  - CVD reactor configuration
  - CVD reactor summary
- Atmospheric Pressure CVD, APCVD
- Low Pressure CVD, LPCVD
- Plasma-Assisted CVD
- Plasma-Enhanced CVD, PECVD
- High-Density Plasma CVD, HDPCVD
## CVD Reactor Types

<table>
<thead>
<tr>
<th>CVD Reactor Types</th>
<th>Atmospheric</th>
<th>Low-pressure</th>
<th>Batch</th>
<th>Single-wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hot-wall</td>
<td>√</td>
<td>√</td>
<td>√</td>
<td></td>
</tr>
<tr>
<td>Cold-wall</td>
<td>√</td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Continuous motion</td>
<td>√</td>
<td></td>
<td>√</td>
<td></td>
</tr>
<tr>
<td>Epitaxial</td>
<td>√</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plenum</td>
<td>√</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nozzle</td>
<td>√</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Barrel</td>
<td>√</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cold-wall planar</td>
<td></td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Plasma-assisted</td>
<td></td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Vertical-flow Isothermal</td>
<td></td>
<td>√</td>
<td></td>
<td>√</td>
</tr>
</tbody>
</table>
### Types of CVD Reactors and Principal Characteristics

<table>
<thead>
<tr>
<th>Process</th>
<th>Advantages</th>
<th>Disadvantages</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>APCVD (Atmospheric Pressure CVD)</td>
<td>Simple reactor, fast deposition, low temperature.</td>
<td>Poor step coverage, particle contamination, and low throughput.</td>
<td>Low-temperature oxides (both doped and undoped).</td>
</tr>
<tr>
<td>LPCVD (Low Pressure CVD)</td>
<td>Excellent purity and uniformity, conformal step coverage, large wafer capacity.</td>
<td>High temperature, low deposition rate, more maintenance intensive and requires vacuum system.</td>
<td>High-temperature oxides (both doped and undoped), silicon nitride, polysilicon, W, WSi₂.</td>
</tr>
<tr>
<td>Plasma Assisted CVD:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>β Plasma Enhanced CVD (PECVD)</td>
<td>Low temperature, fast deposition, good step coverage, good gap fill.</td>
<td>Requires RF system, higher cost, stress is much higher with a tensile component, and chemical (e.g., H₂) and particle contamination.</td>
<td>High aspect ratio gap fill, low-temperature oxides over metals, ILD-1, ILD, copper seed layer for dual damascene, passivation (nitride).</td>
</tr>
<tr>
<td>β High Density Plasma CVD (HDPCVD)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Continuous-Processing APCVD Reactors

(a) Gas-injection type

(b) Plenum type

Figure 11.12
Excellent Step Coverage of APCVD TEOS-O3

Trench fill by chemical vapor deposition

TEOS-O3

Trench CVD oxide

Liner oxide

Nitride

n-well

p-well

p^- Epitaxial layer

p^+ Silicon substrate
Planarized Surface after Reflow of PSG

Before reflow

After reflow

Metal or polysilicon

PSG
LPCVD Reaction Chamber for Deposition of Oxides, Nitrides, or Polysilicon

Three-zone heating element

Spike thermocouples (external, control)

Profile thermocouples (internal)

Exhaust to vacuum pump

Gas inlet

Pressure gauge

Figure 11.16
Oxide Deposition with TEOS LPCVD

Figure 11.17
Doped Polysilicon as a Gate electrode

Figure 11.18
Advantages of Plasma Assisted CVD

1. Lower processing temperature (250 – 450°C).
2. Excellent gap-fill for high aspect ratio gaps (with high-density plasma).
3. Good film adhesion to the wafer.
4. High deposition rates.
5. High film density due to low pinholes and voids.
6. Low film stress due to lower processing temperature.
Film Formation during Plasma-Based CVD

1) Reactants enter chamber
2) Dissociation of reactants by electric fields
3) Film precursors are formed
4) Adsorption of precursors
5) Precursor diffusion into substrate
6) Surface reactions
7) Desorption of by-products
8) By-product removal

Figure 11.19
General Schematic of PECVD for Deposition of Oxides, Nitrides, Silicon Oxynitride or Tungsten

Figure 11.20
## Properties of Silicon Nitride for LPCVD Versus PECVD

<table>
<thead>
<tr>
<th>Property</th>
<th>LPCVD</th>
<th>PECVD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition temperature (°C)</td>
<td>700 – 800</td>
<td>300 – 400</td>
</tr>
<tr>
<td>Composition</td>
<td>Si$_3$N$_4$</td>
<td>Si$_x$N$_y$H$_z$</td>
</tr>
<tr>
<td>Step coverage</td>
<td>Fair</td>
<td>Conformal</td>
</tr>
<tr>
<td>Stress at 23°C on silicon (dyn/cm$^2$)</td>
<td>1.2 – 1.8 x 10$^{10}$</td>
<td>1 – 8 x 10$^9$</td>
</tr>
<tr>
<td></td>
<td>(tensile)</td>
<td>(tensile or compressive)</td>
</tr>
</tbody>
</table>
High Density Plasma Deposition Chamber

- Popular in mid-1990s
- High density plasma
- Highly directional due to wafer bias
- Fills high aspect ratio gaps
- Backside He cooling to relieve high thermal load
- Simultaneously deposits and etches film to prevent bread-loaf and key-hole effects

Photograph courtesy of Applied Materials, Ultima HDPCVD Centura
Five Steps of HDPCVD Process

1. Ion-induced deposition
2. Sputter etch
3. Redeposition
4. Hot neutral CVD
5. Reflection
Dep-Etch-Dep Process

Film deposited with PECVD creates pinch-off at the entrance to a gap resulting in a void in the gap fill.

1) Ion-induced deposition of film precursors

2) Argon ions sputter-etch excess film at gap entrance resulting in a beveled appearance in the film.

3) Etched material is redeposited. The process is repeated resulting in an equal “bottom-up” profile.
3-Part Process for Dielectric Gap Fill

1) HDPCVD gap fill

2) PECVD cap

3) Chemical mechanical planarization
Effects of Keyholes in ILD on Metal Step Coverage

Keyhole defect in interlayer dielectric

Aluminum

SiO₂

a) SiO₂ deposited by PECVD

b) SiO₂ is planarized

Metal void caused by keyhole defect in SiO₂

c) Next layer of aluminum is deposited
Dielectrics and Performance

• Dielectric Constant
• Gap Fill
• Chip Performance
• Low-k Dielectric
• High-k Dielectric
• Device Isolation
  – LOCOS
  – STI
## Potential Low-\( k \) Materials for ILD of ULSI Interconnects

<table>
<thead>
<tr>
<th>Potential low-( k ) Dielectric</th>
<th>Dielectric Constant ( (k) )</th>
<th>Gap Fill ( (\mu m) )</th>
<th>Cure Temp. ( (^\circ C) )</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSG (silicon oxyfluoride, ( Si_3O_F_y ))</td>
<td>3.4 – 4.1</td>
<td>&lt;0.35</td>
<td>No issue</td>
<td>FSG has almost the same ( k )-value as ( SiO_2 ) and reliability concern that fluorine will attack and corrode tantalum barrier metal.</td>
</tr>
<tr>
<td>HSQ (hydrogen silsesquioxane)</td>
<td>2.9</td>
<td>&lt;0.10</td>
<td>350 – 450</td>
<td>Silicon-based resin polymer available in solution as Fox (Flowable Oxide) for spin-on coating application. May require surface passivation to reduce moisture absorption. Cure is done in nitrogen.</td>
</tr>
<tr>
<td>Nanoporous silica</td>
<td>1.3 – 2.5</td>
<td>&lt;0.25</td>
<td>400</td>
<td>Inorganic material with tunable dielectric constant that relies on pore density. Increased porosity reduces mechanical integrity – porous material must withstand polishing, etching and heat treatments without degradation.</td>
</tr>
<tr>
<td>Poly(arylene) ether (PAE)</td>
<td>2.6 – 2.8</td>
<td>&lt;0.15</td>
<td>375 – 425</td>
<td>Spin-on aromatic polymer with excellent adhesion and ability to be polished with CMP.</td>
</tr>
<tr>
<td>a-CF (fluorinated amorphous carbon or FLAC)</td>
<td>2.8</td>
<td>&lt;0.18</td>
<td>250 – 350</td>
<td>Leading candidate for CVD deposition with high density plasma CVD (HDPCVD) to produce film with good thermal stability and adhesion.</td>
</tr>
<tr>
<td>Parylene AF4 (aliphatic tetrafluorinated poly-p-xylylene)</td>
<td>2.5</td>
<td>&lt;0.18</td>
<td>420 – 450</td>
<td>CVD film that meets adhesion and via resistance requirements with need to maintain gas delivery system at 200(^\circ)C to control parylene precursor flow rate.</td>
</tr>
</tbody>
</table>

---

Interconnect Delay (RC) vs. Feature Size (µm)

- Interconnect delay (RC)
- Gate delay

Figure 11.24

Semiconductor Manufacturing Technology
by Michael Quirk and Julian Serda

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Total Interconnect Wiring Capacitance

Redrawn with permission from Semiconductor International, September 1998
## Low-\(k\) Dielectric Film Requirements

<table>
<thead>
<tr>
<th>Electrical</th>
<th>Mechanical</th>
<th>Thermal</th>
<th>Chemical</th>
<th>Processing</th>
<th>Metallization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low dielectric constant</td>
<td>Good adhesion</td>
<td>Thermal stability</td>
<td>Resistant: acids and bases</td>
<td>Patterningability</td>
<td>Low contact resistance</td>
</tr>
<tr>
<td>Low dielectric loss</td>
<td>Low shrinkage</td>
<td>Low coefficient of thermal expansion</td>
<td>Etch selectivity</td>
<td>Good gap fill</td>
<td>Low electromigration (corrosion)</td>
</tr>
<tr>
<td>Low leakage</td>
<td>Crack resistant</td>
<td>High conductivity</td>
<td>Low impurities</td>
<td>Planarization</td>
<td>Low stress voiding</td>
</tr>
<tr>
<td>High reliability</td>
<td>Low stress</td>
<td>No corrosion</td>
<td>Low pin hole</td>
<td>Hillock (smooth surface)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Good hardness</td>
<td>Low moisture uptake</td>
<td>Low particulate</td>
<td>Compatible with barrier metals (Ta, TaN, TiN, etc.)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Storage life</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
General Diagram of DRAM Stacked Capacitors

- SiO₂ dielectric
- Doped polysilicon capacitor plate
- Buried contact diffusion
- Doped polysilicon capacitor plate
Shallow Trench Isolation

Photograph courtesy of Integrated Circuit Engineering
Spin-on Dielectrics

- Spin-on Glass (SOG)
- Spin-on Dielectric (SOD)
- Epitaxy
  - Epitaxy growth methods
    - Vapor-phase epitaxy
    - Metalorganic CVD
    - Molecular-beam epitaxy
Gap-Fill with Spin-On-Glass (SOG)

1) Initial SOG gap fill
2) SOG after curing
3) CVD oxide cap
## Proposed HSQ Low-

### Dielectric Processing Parameters

<table>
<thead>
<tr>
<th>Major Operation</th>
<th>Process Step</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Spin coating</strong></td>
<td>Apply bowl speed</td>
<td>50 rpm</td>
</tr>
<tr>
<td></td>
<td>Maximum bowl speed</td>
<td>800 – 1500 rpm</td>
</tr>
<tr>
<td></td>
<td>Backside rinse</td>
<td>800 rpm, 5 sec</td>
</tr>
<tr>
<td></td>
<td>Topside edge bead removal</td>
<td>1000 rpm, 10 sec</td>
</tr>
<tr>
<td></td>
<td>Spin Dry</td>
<td>1000 rpm, 5 sec</td>
</tr>
<tr>
<td><strong>Cure</strong></td>
<td>Initial soft-bake cure</td>
<td>200°C, 60 sec, N₂ purge</td>
</tr>
<tr>
<td></td>
<td>In-line cure</td>
<td>475°C, 60 sec, N₂ ambient</td>
</tr>
</tbody>
</table>
Epitaxy

- Epitaxy Growth Model
- Epitaxy Growth Methods
  - Vapor-Phase Epitaxy (VPE)
  - Metalorganic CVD (MOCVD)
  - Molecular-Beam Epitaxy (MBE)
Silicon Epitaxial Growth on a Silicon Wafer

Chemical reaction

By-products

Deposited silicon

Epitaxial layer

Single silicon substrate